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A Logic State Analyzer for Microprocessor Systems

A new logic state analyzer for debugging systems that use popular microprocessors has broadly expanded triggering capabilities plus keyboard control and mnemonic display that help solve problems more efficiently.

by Jeffrey H. Smith

WITH A LOGIC STATE ANALYZER displaying the operation of his state machine, the digital designer is able to locate faults quickly and conveniently whether they are in hardware, in software (or firmware), or in the manner that hardware and software interface. The logic state analyzer, introduced by Hewlett-Packard in 1973,[1] captures a sequence of digital words and displays the words in tabular form just as a synchronous system "sees" them. Data is sampled by a clock from the system running at its normal speed and is displayed as a list showing the sequential flow of states.

The recent precipitous decrease in the per-part price of microprocessors has created an explosive growth in their use. Compared with a ROM-controlled state machine, or even most discrete-logic processors of a few years ago, today's microprocessor system—with its easily implemented interrupts, subroutine capability, and multiple addressing modes—executes highly complex programs. This has generated a need for a logic state analyzer optimized for analyzing microprocessor operation.

Because of the quantity and the complexity of the data that must be handled, such an analyzer should have far more sophisticated means of trigger-point selection and storage qualification than earlier analyzers. For example, it is normal for a sequence of instructions to be repeated many times in the form of a loop, yet the designer may be interested in only the 10th or the 100th occurrence of this sequence. Or, the user may be interested in examining activity at a specific address, such as a RAM location used to store a status flag, only when it is written from a specific segment of his program.

Even if usages of this complexity had been anticipated when the first analyzers were designed, it is doubtful that all of the needed trigger capability could have been added because of constraints imposed by mechanical and ergonomic considerations. For example, most present analyzers use a row of 16 three-position (1, OFF, 0) toggle switches to select a 16-bit trigger word. These switches perform the twin functions of selecting the trigger word and indicating what it is—adequate if only one word is required. This row of switches occupies about 6 square inches of panel area, however, and additional trigger words would each add 6 square inches and 16 controls to the panel.

Fortunately, the microprocessor, which generated the need for a new type of analyzer, has also provided a solution to the problems of implementing it in a form that is both convenient to use and possible to build. Adding an additional trigger word to a microprocessor-controlled keyboard instrument requires the addition of, at most, only one control (a key to select the trigger), and the allocation of a fraction of

Cover: *There is no functional relationship between these two instruments–a fetal monitor for obstetrics and a logic state analyzer for digital electronics–but both share a basic design objective: operating simplicity, even though the instruments perform their intended functions in a highly sophisticated manner. Articles in this issue include descriptions of the different approaches taken.*

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Fig. 1. *Model 1611A Logic State Analyzer, designed to test systems using popular microprocessors, captures and displays the sequential flow of states on a microprocessor's* DATA *and* ADDRESS *busses and at up to eight other nodes selected by the user.*

a line on the display to indicate the trigger selected. The use of a microprocessor as a controller allows much of an instrument's complexity to remain invisible to the user.

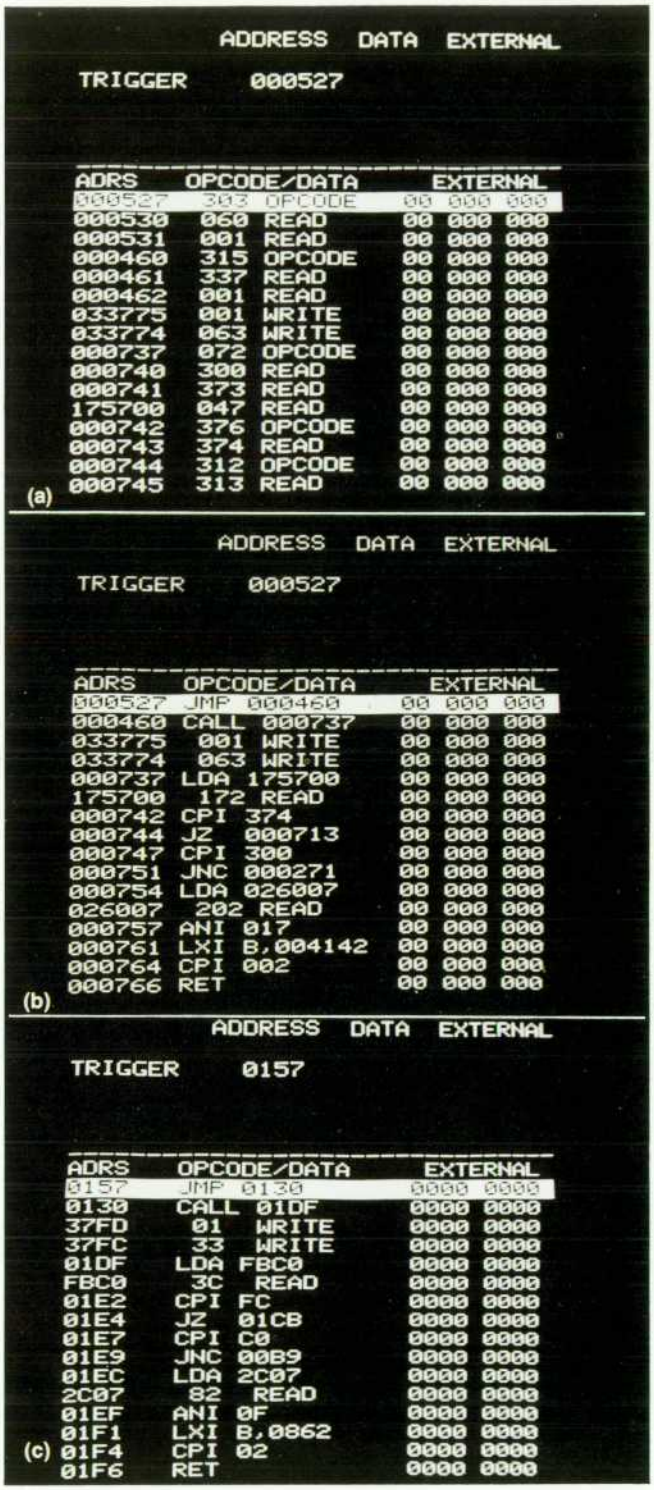
A New Analyzer

An internal 8-bit MOS microprocessor is used as a controller in a new logic state analyzer, the Hewlett-Packard Model 1611A (Fig. 1). The analyzer is keyboard controlled and a CRT displays both the measurement set-up information and the measurement results. Intended specifically to aid in the design and troubleshooting of microprocessor-based systems, it has far more extensive triggering options than are presently available in other logic state analyzers.

Besides making a complex machine seem relatively "friendly" to the user, this new analyzer's internal microprocessor gives the instrument sufficient intelligence to display the results of its measurements in several formats. The contents of the ADDRESS bus and the DATA bus of the microprocessor being monitored may be displayed in either the octal or the hexadecimal number base (Fig. 2). If desired, the DATA bus contents may also be decoded into the mnemonic set used by the microprocessor in the system being tested. This is an extremely important feature for a microprocessor monitor since a person examining system operation is usually interested in seeing a flow of information, rather than detecting the existence of isolated, individual states. He will frequently want to scan large blocks of code rapidly where converting mentally from raw data to machine code could be very time-consuming. Indeed, a software writer, using an assembler, may have never worked with the octal or hexadecimal representation of his code. With a mnemonic display, he may rapidly scan blocks of data to determine if his code is executing properly. If a problem is spotted, the display may be converted to an absolute listing in either octal or hexadecimal for a more detailed, step-by-step examination of program execution.

Mnemonic display is made possible by designing the new logic-state analyzer to accept "personality" modules that configure it to monitor specific microprocessors. Included in a personality module is a ROM that stores the mnemonic set of the microprocessor for which the module is tailored. Presently, personality modules are available for two of the most popular 8-bit processors, the 8080 and the 6800. Other modules are under development.

Connecting large numbers of individual probes to a circuit to be monitored is one of the greatest sources of error and inconvenience associated with the use of a logic state analyzer. The new analyzer's use of a personality module allows each module to include



```
(a)
                ADDRESS   DATA   EXTERNAL

TRIGGER         000527

ADRS    OPCODE/DATA          EXTERNAL
000527   303 OPCODE          00 000 000
000530   060 READ            00 000 000
000531   001 READ            00 000 000
000460   315 OPCODE          00 000 000
000461   337 READ            00 000 000
000462   001 READ            00 000 000
033775   001 WRITE           00 000 000
033774   063 WRITE           00 000 000
000737   072 OPCODE          00 000 000
000740   300 READ            00 000 000
000741   373 READ            00 000 000
175700   047 READ            00 000 000
000742   376 OPCODE          00 000 000
000743   374 READ            00 000 000
000744   312 OPCODE          00 000 000
000745   313 READ            00 000 000

(b)
                ADDRESS   DATA   EXTERNAL

TRIGGER         000527

ADRS    OPCODE/DATA          EXTERNAL
000527   JMP 000460          00 000 000
000460   CALL 000737         00 000 000
033775    001 WRITE          00 000 000
033774    063 WRITE          00 000 000
000737   LDA 175700          00 000 000
175700    172 READ           00 000 000
000742   CPI 374             00 000 000
000744   JZ  000713          00 000 000
000747   CPI 300             00 000 000
000751   JNC 000271          00 000 000
000754   LDA 026007          00 000 000
026007    202 READ           00 000 000
000757   ANI 017             00 000 000
000761   LXI B,004142        00 000 000
000764   CPI 002             00 000 000
000766   RET                 00 000 000

(c)
                ADDRESS   DATA   EXTERNAL

TRIGGER         0157

ADRS    OPCODE/DATA          EXTERNAL
0157     JMP 0130            0000 0000
0130     CALL 01DF           0000 0000
37FD      01  WRITE          0000 0000
37FC      33  WRITE          0000 0000
01DF     LDA FBC0            0000 0000
FBC0      3C  READ           0000 0000
01E2     CPI FC              0000 0000
01E4     JZ  01CB            0000 0000
01E7     CPI C0              0000 0000
01E9     JNC 00B9            0000 0000
01EC     LDA 2C07            0000 0000
2C07      82  READ           0000 0000
01EF     ANI 0F              0000 0000
01F1     LXI B,0862          0000 0000
01F4     CPI 02              0000 0000
01F6     RET                 0000 0000
```

Fig. 2. *Binary information appearing on a microprocessor's* DATA *and* ADDRESS *buses may be displayed in a variety of formats to facilitate analysis. The photo at top (a) shows a data sequence presented in the octal format. In the center photo (b), the same sequence is presented in the mnemonic set of the microprocessor (an 8080). Because each mnemonic instruction may involve more than one memory transaction, the displayed table is a condensation and thus represents a longer sequence than that shown in (a). The sequence shown in (c) is the same as that in (b) but the addresses are listed in the hexadecimal format.*

probes whose voltage threshold limits, pin connections, and clock slope are designed to match the microprocessor being monitored. The analyzer's probes connect quickly to the microprocessor by means of a clothespin-style 40-pin DIP clip or by means of a low-profile 40-pin male plug (Fig. 3). In addition to the 40-pin microprocessor probe, the new analyzer has a conventional 8-input probe. This probe may be used to monitor up to eight TTL-level signals that may not be accessible at the microprocessor.

Versatile Triggering

The new Model 1611A Analyzer uses a 32-bit TRIGGER that is divided into three distinct fields: a 16-bit ADDRESS field, an 8-bit DATA BUS field (expandable to 16 bits) and the eight lines of information monitored by the EXTERNAL probe. The user of the 1611A may specify the trigger ADDRESS as either a simple, single address "breakpoint" or he may use the operators $\geq$ and $\leq$ to define a range of addresses as the trigger point. For example, all addresses between 1000 and 2000 could be selected. The EXTERNAL trigger word is entered in binary with a "don't-care" (OFF) option on each bit so that individual inputs may be turned off if the desired trigger word is less than eight bits wide. Any part of any field may also be set to don't care (OFF) if desired.

Multiple passes through loops and subroutines or multiple accesses to a memory location may be examined using the analyzer's TRIGGER OCCURRENCE counter. This holds off trigger recognition until the specified number of triggers has been encountered.

Windowed triggering permits the analyzer to search for a sequence of two trigger words or to search for a trigger word within a limited portion of a microprocessor's program execution. ADDRESS, DATA BUS, and EXTERNAL words may be entered to define a TRIGGER ENABLE event. The arming of the trigger is now inhibited until the ENABLE event occurs. A similar 3-field TRIGGER DISABLE event may be selected to disarm the search for a trigger. This causes the TRIGGER comparator to look for a trigger only between the ENABLE and DISABLE points.

Selective Data Gathering

The new analyzer has four different run modes. TRACE results in a display of sequential program steps, starting at the selected trigger point. A PRE-TRIGGER of up to 63 program steps may be selected. This causes states prior to the trigger point to be displayed (Fig. 4a). Using this feature, it is possible to trigger on a fault condition and examine the code leading up to the fault. If post-trigger data is of interest, a DELAY of up to 65,472 steps after the trigger event may be specified.

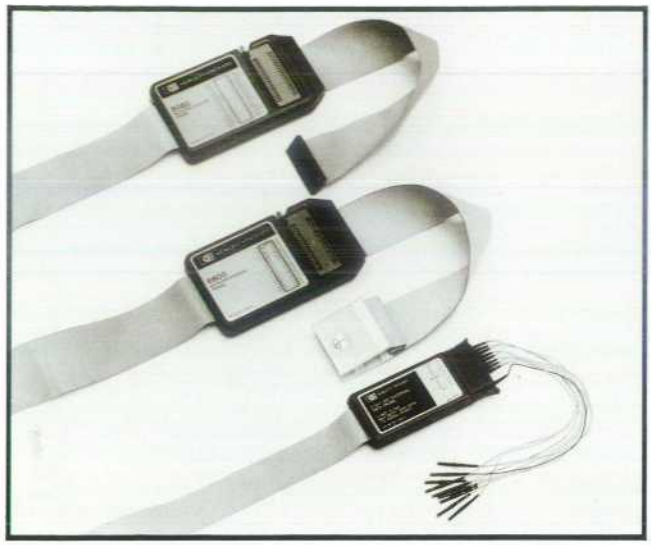


Fig. 3. *Probing arrangement allows direct connection to a microprocessor with a "clothespin" clip (center) or, if space is limited, by plugging the connector on the end of the cable (top) into the microprocessor socket and plugging the microprocessor into the probe body. The* EXTERNAL *connections are through separate leads (bottom). These may plug directly on to test pins, or they may be inserted in pincher-type miniature probes (see Fig. 1).*

The TRACE TRIGGERS mode is essentially a selective store—the analyzer stores only the events that meet the TRIGGER specification. With this mode, it is possible to examine activity of only a certain part of a microprocessor's program execution, for example, all reads from a specific I/O port, all JSR instructions, or all writes to RAM (Fig. 4b). Because events are "qualified" before they are stored, only those events of interest are retained, resulting in a significant savings in the time required to analyze the results of a measurement. Only an absolute display (no mnemonics) is offered in this mode since the code segments or memory operations stored may not be consecutive or even related.

Two counting modes are incorporated. TIME INTERVAL gives the time (with a resolution of 1 microsecond) between the TRIGGER ENABLE and the TRIGGER DISABLE points (Fig. 5a).The maximum count is 2^{24} microseconds or slightly more than 16 seconds. COUNT TRIGGERS gives the number of times that the TRIGGER specification is found within this range (Fig. 5b). These modes are useful for measuring the execution time or the coding efficiency of segments of a microprocessor program.

Seizing Control

To examine the hardware operation associated with a segment of code in detail, it is frequently desirable to halt the operation of a processor. The 1611A has a provision to do this by means of an open-collector gate driving the tested microprocessor's HALT or READY line. This gate is driven by the trigger circuits within the 1611A and can either halt the test system when the capture memory internal to the 1611A is full, or it can cause the system under test to single step once each time the TRACE key is depressed. Thus, the processor may be halted at a specific trigger point in its program each time that trigger occurs, or it may be single stepped beginning at the trigger point. In either case, the analyzer displays the code executed in either absolute or mnemonic format.

The new 1611A, like most logic state analyzers, is primarily a functional test instrument, that is, it is best at determining whether or where a malfunction occurs. The cause of the error is frequently obvious if its nature and location are known. If the cause is not

(a)

ADRS	OPCODE/DATA		EXTERNAL
		ADDRESS DATA	EXTERNAL
TRIGGER	0157		
		PRE-TRIGR=10	
34D2	1F	WRITE	0000 0000
097B	2C	OPCODE	0000 0000
097C	BE	OPCODE	0000 0000
34D3	1F	READ	0000 0000
097D	C2	OPCODE	0000 0000
097E	7A	READ	0000 0000
097F	09	READ	0000 0000
0980	C9	OPCODE	0000 0000
37FC	57	READ	0000 0000
37FD	01	READ	0000 0000
0157	C3	OPCODE	0000 0000
0158	30	READ	0000 0000
0159	01	READ	0000 0000
0130	CD	OPCODE	0000 0000
0131	DF	READ	0000 0000
0132	01	READ	0000 0000

(b)

ADRS	OPCODE/DATA		EXTERNAL
		ADDRESS DATA	EXTERNAL
TRIGGER	<= 37FF		
	>= 3700		
TRIGGER STORE			
37FA	87	READ	0000 0000
37FB	09	READ	0000 0000
37FC	57	READ	0000 0000
37FD	01	READ	0000 0000
37FD	01	WRITE	0000 0000
37FC	33	WRITE	0000 0000
37FC	33	READ	0000 0000
37FD	01	READ	0000 0000
3767	01	READ	0000 0000
37FD	01	WRITE	0000 0000
37FC	57	WRITE	0000 0000
37FB	09	WRITE	0000 0000
37FA	87	WRITE	0000 0000
37FA	87	READ	0000 0000
37FB	09	READ	0000 0000
37FC	57	READ	0000 0000

Fig. 4. *States leading up to a trigger word may be displayed showing how a program gets to a particular state (a). In this example, a pre-trigger display of 10 states was selected. The trigger word (0157) is displayed in inverse video. In* TRACE TRIGGERS *mode (b), only those states meeting specified trigger conditions are captured for display, in this case states having hexadecimal addresses between 3700 and 37FF.*

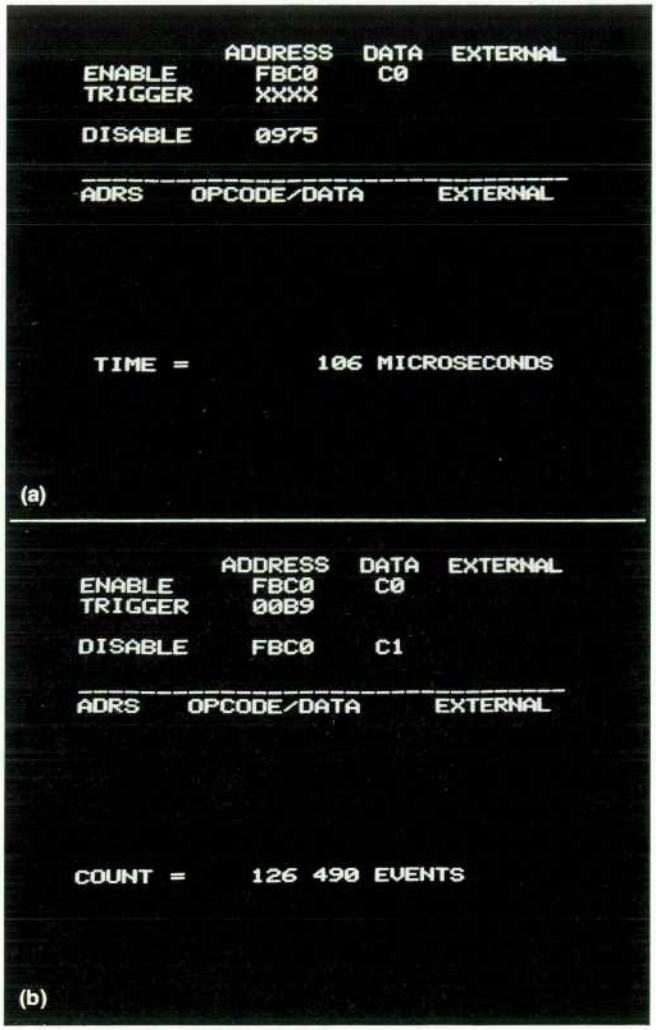


Fig. 5. *When operating in the TIME INTERVAL mode (a), Model 1611A measures the execution time from one point in a program (selected by TRIGGER ENABLE) to another point (TRIGGER DISABLE). In the COUNT TRIGGERS mode (b) the instrument counts the number of times a particular address (00B9) is accessed between ENABLE and DISABLE points, in this case through a loop beginning and ending at address FBC0.*

obvious, it is usually necessary to either make additional measurements with the logic state analyzer or to monitor the system with considerably greater resolution than that provided by present analyzers. As an example, 5-ns, or even 1-ns glitches and pulse overlaps can wreak havoc with the operation of the TTL circuits commonly used with processors. To facilitate the measurement of fast signals, the 1611A provides a TTL-level output pulse for an oscilloscope or other high-resolution instrument every time that the 1611A finds its TRIGGER word. One pulse each run is available from another output in case that it is necessary to trigger on the specific event recognized by the 1611A. This second output may also be used as a synchronized stimulus to the system being monitored in order to observe its response to an external event.

Self-Check

The 1611A has two means of verifying that it is in proper operating condition. When its power is turned on, it executes a software routine that checks itself internally and displays error messages to indicate any problems it finds. Since the probes and some of the data acquisition circuits cannot be tested by software, the microprocessor analyzer has a PROBE TEST socket that simulates, in hardware, the signals generated by a microprocessor. These signals are analogous to the signals present at the calibrator jack of an oscilloscope and generate an easily recognizable pattern on the display when correctly read by the probe.

System Organization

Fig. 6 shows a simplified block diagram of the new analyzer. Signals appearing on the microprocessor's pins and the eight external lines are monitored by buffered probes and clocked into a temporary storage register within the personality module. The personality module converts the data into the parallel format required by the input data bus and provides signals ($\overline{\text{COMPARE}}$ and $\overline{\text{STORE}}$) to the comparator and data acquisition memory that indicate when the storage buffer contains new, valid data. Four flag lines contain additional information of use to the 1611A's mnemonic decode program, such as when the data bus contents represent an instruction op code or whether a byte represents a READ or a WRITE. This input data bus is completely separate from the 1611A's internal microprocessor bus so that its data acquisition rate is not limited by the speed of the internal MOS processor.

The 1611A uses the same concepts used in previous Hewlett-Packard logic state analyzers[1,2] with the exception that the comparators, counters, and acquisition memory are under microprocessor control. The output of the temporary storage register is continuously clocked into a 36-bit wide by 64-byte deep shift-register-like memory.

When a trigger point is found, a count is entered into the 8-bit OCCURRENCE counter. When this counter counts out, a 16-bit DELAY counter is enabled and it starts counting memory cycles of the microprocessor being monitored. When the DELAY counter overflows, further storage of data into memory is inhibited and flags are set that are read by the 1611A's internal microprocessor to indicate that a data acquisition cycle is complete. The internal microprocessor unloads memory, converts the data as requested from the keyboard and writes the result to the display.

In the COUNT and TIME modes of operation, the OCCURRENCE and DELAY counters are combined into one 24-bit counter that counts the TRIGGER comparator output in the COUNT TRIGGERS mode and counts an internal crystal-controlled reference in the TIME IN-

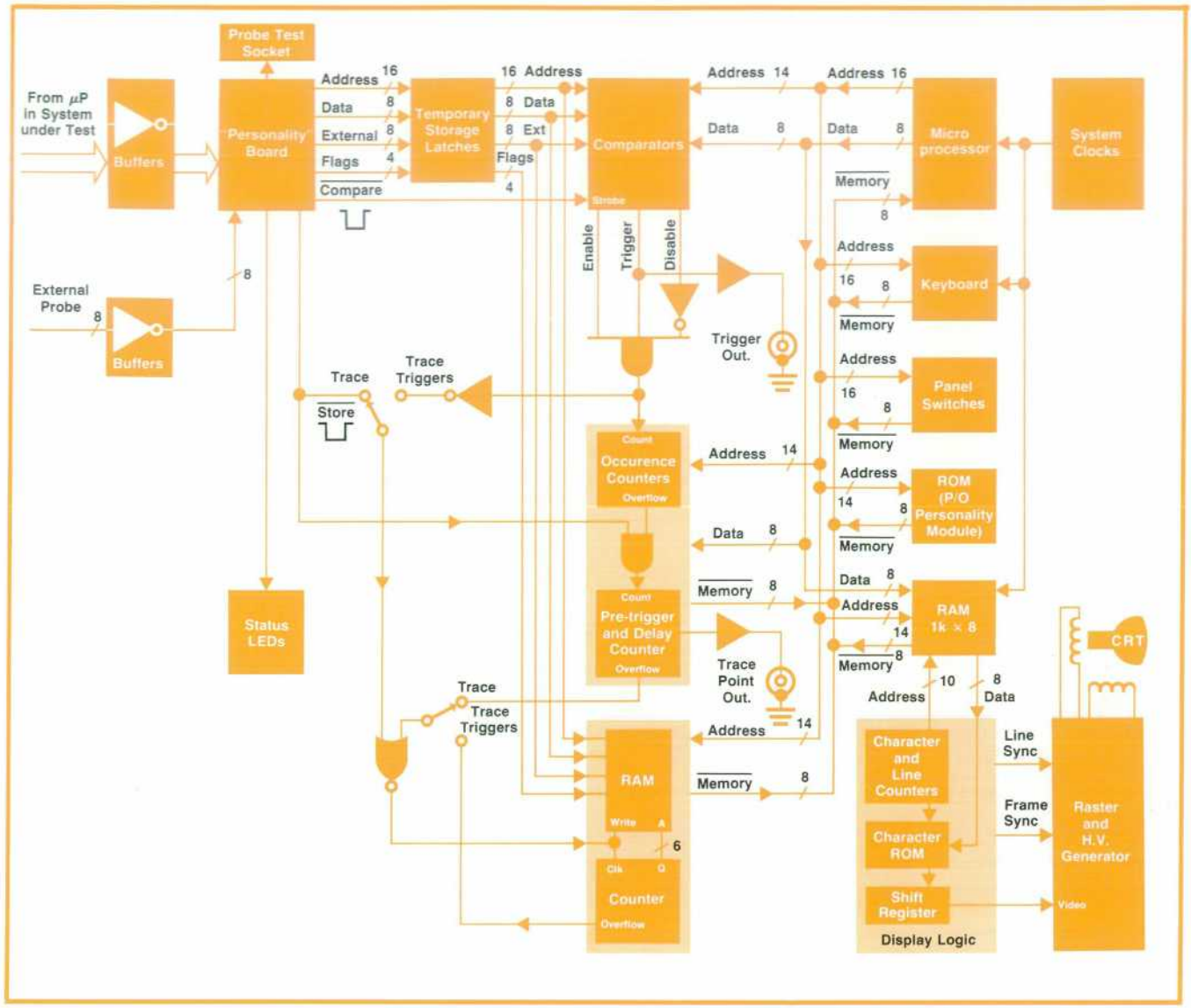


Fig. 6. *Simplified block diagram of Model 1611A Logic State Analyzer.*

TERVAL mode (gating for the COUNT and TIME modes of operation is not shown in the simplified block diagram).

All of the internal functions within the 1611A are addressed as memory from an internal bus. As an example, the contents of the counters are determined by performing memory reads at the counter addresses, and the counters are loaded by performing memory writes. This internal bus structure is conventional with the exception that the data bus is split into two unidirectional busses (DATA and $\overline{\text{MEMORY}}$) in order to simplify the problems of bus turnaround. The DATA bus handles all data outgoing from the microprocessor and the $\overline{\text{MEMORY}}$ bus contains all incoming data.

Each of the contactless, ferrite core keyswitches in the keyboard is assigned a position in a matrix of eight columns and six rows (Fig. 7). The matrix is scanned, one key at a time, by a 6-bit counter. When a depressed key is detected, the count is inhibited and the counter holds the keycode of the depressed key. At the same time, two flags are set. KEY DOWN indicates that a key is depressed while KEY UNREAD is set when a key is first depressed and is cleared by hardware after the keyboard is read.

The keyboard is assigned a memory address so that it may be read by the 1611A's microprocessor as one 8-bit word—the 2 flags and the 6-bit counter output. If both flags are low, no keys are depressed and the keycode is ignored. If both flags are high, a new key has been depressed and the counter output represents its keycode. If KEY DOWN is high and KEY UNREAD is low, the counter output represents a key that has been read but that is still being held down. No keyboard memory is required since the keyboard is read approximately every 160μs—much faster than data can

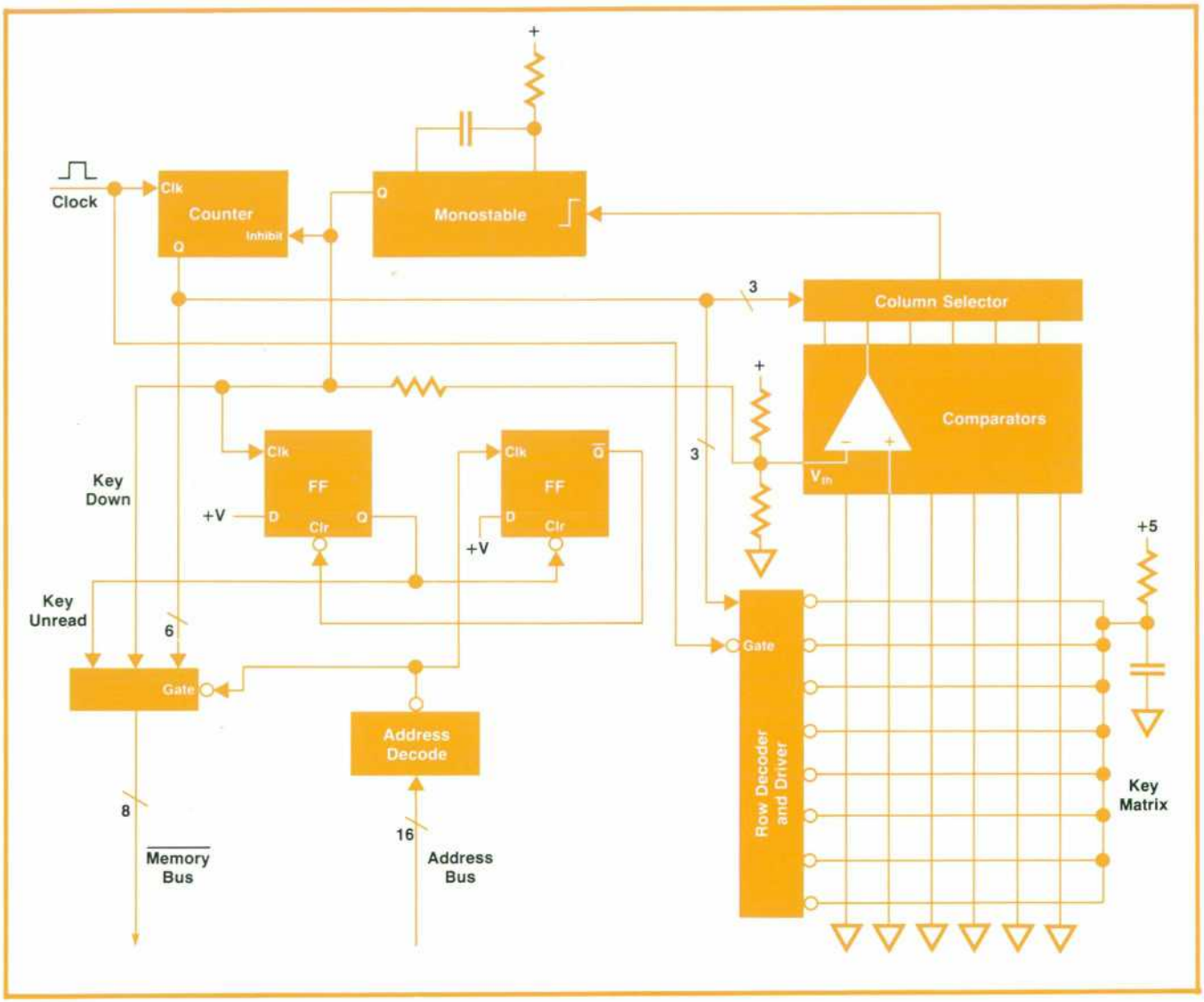


Fig. 7. *Block diagram of the keyboard scanner. The keyboard is assigned an address in the instrument's memory and is read once every 160 μs. The two flags (KEY DOWN and KEY UNREAD) indicate to the instrument's microprocessor whether or not any action should be taken on the 6-bit key code presented to the memory bus.*

be entered manually. Hysteresis is introduced by means of the connection between KEY DOWN and the comparator threshold so that a slow key depression does not result in double triggering.

Trigger Recognition

The many triggering modes of the 1611A were made possible by the development of a new form of trigger recognizer. A conventional bit comparator of the kind usually used to perform this function is shown in Fig. 8a. This has the three functions necessary to recognize a trigger—storage of the reference word, comparison, and enabling—performed separately. With TTL circuits this trigger recognizer requires about one DIP pack of circuitry per bit. Since the 1611A trigger recognizer contains over 100 bits of comparison, an enormous number of packs would have been required to implement it by conventional means.

A multi-bit trigger comparator may be implemented in one pack by using a static RAM as a comparator, as shown in Fig. 8b. Since there is a one-to-one correspondence between RAM cells and any digital word presented to its address lines, any pattern may be searched for by loading the proper mask into the RAM by means of the instrument's internal address and data buses. Note that one RAM can simultaneously search the input data for several conditions. The RAM shown in the figure produces a true signal at output 0 if the input = 8_{16}, a true output at output 1 if the input = $X000_2$(X = don't care) and a true signal at output 2 if the input

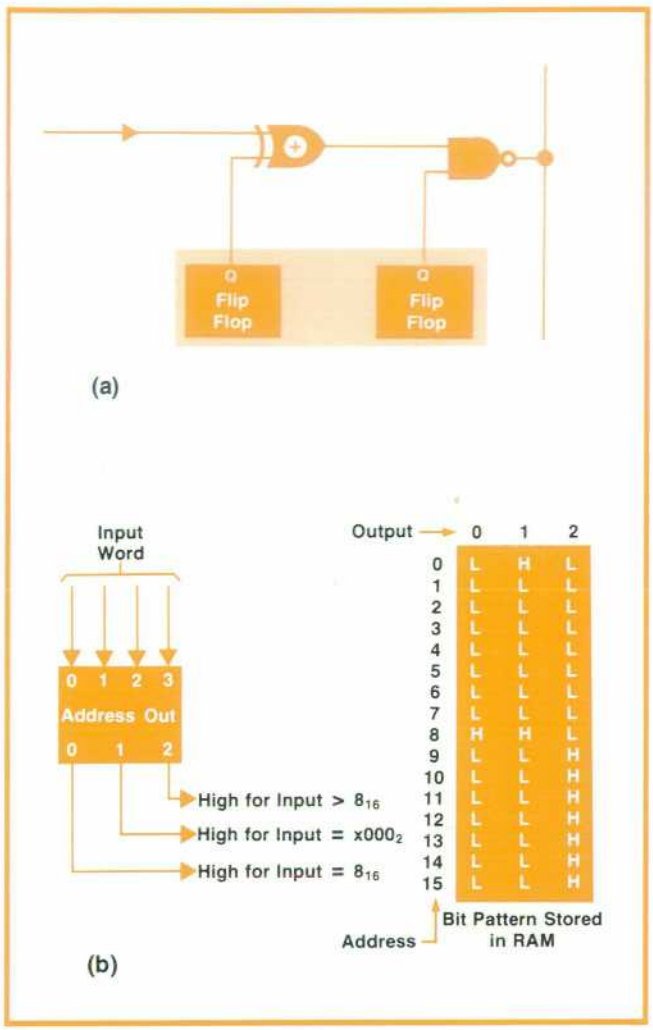


Fig. 8. *Conventional bit comparator (a) separately implements storage of the reference bit, comparison, and enabling. Each bit in a word requires the circuitry shown here. A single RAM can be used as a multi-bit comparator (b) by loading the appropriate bit pattern (mask) into it, as shown by the table in this example.*

word is greater than 8_{16}.

The above suggests an elegant technique for making range comparisons on very wide digital numbers. The comparator diagrammed in Fig. 9 returns a high output if word A (the comparator input) is equal to or greater than word B (the mask stored in the RAM). The word is tested in 4-bit increments. If the most significant four bits of A are greater in magnitude than the most significant four bits of B, word A must be greater than word B. Similarly, if the most significant bits of A are less than the equivalent bits of B, word A cannot possibly be greater than word B. If these bits of the two words are equal, then a similar test is performed on the next most significant four bits by means of the AND gate logic. This series of tests is repeated, if necessary, until all bits of the two words are tested. Note that all comparisons are made simultaneously in parallel so that there is no intermediate result that must "ripple through" from the most to the least significant bit as with many magnitude comparison techniques. Thus, the comparison time does not increase as the comparator is made wider. If the "greater than" sections of the comparator are loaded with all low states, the circuit defaults to a simple equality comparator.

Display

The 1611A contains a raster-scan, magnetic-deflection CRT display that uses a reliable and inexpensive 7-inch TV-type CRT. It displays up to 24 lines of 32 characters each for a total of 768 characters. Each character is formed by a 5-by-7 matrix of dots. In addition, 1 dot between characters horizontally and 3 dots vertically are always blanked to achieve intercharacter spacing, so each character actually occupies a space 6 dots wide by 10 dots high.

A simplified block diagram of the display logic is shown in Fig. 10. Each character position on screen is

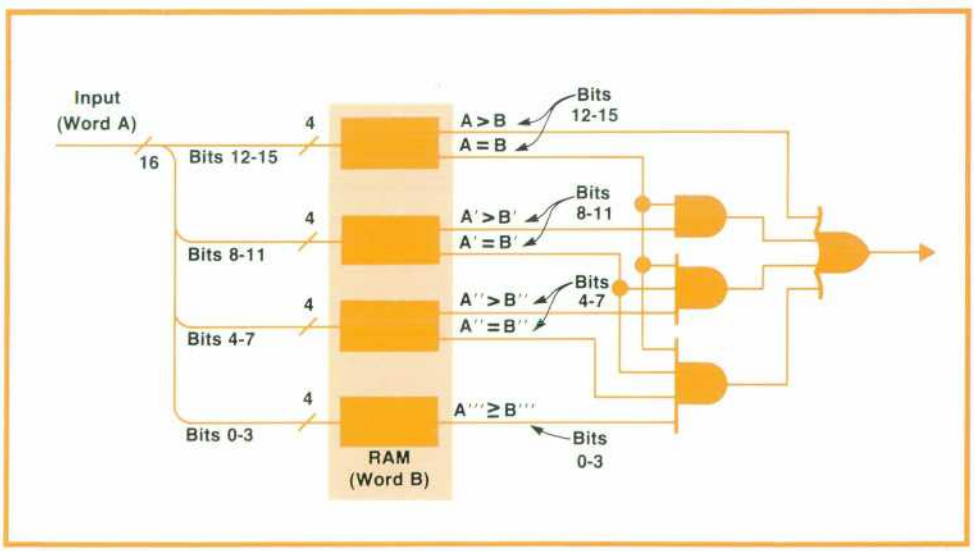


Fig. 9. *A multi-bit comparator for wide digital numbers is implemented with relatively few components using the technique of Fig. 8b.*

assigned a unique location in the 1611A's memory. No line buffer is used as in a conventional raster-scan display. Instead, the RAM is designed to be sufficiently fast so that two memory read or write transactions can be performed during each period of the microprocessor clock. One memory cycle is always available to the microprocessor, if needed. Its output is stored in a latch so that a valid output remains on the MEMORY bus for the remainder of the clock cycle. The other fetch is always used by the display to fetch its next character. By the use of this form of direct memory access, the display circuitry is greatly simplified and neither the display nor the microprocessor is "aware" that the other is using the memory.

The proper pattern of bright and blanked dots is stored in a ROM used to generate each line of each character. Six ROM inputs select one of the 64 characters from the upper-case ASCII character set, and three inputs select one of the seven horizontal scan rows or a blank eighth row. The five outputs of the ROM are loaded into a shift register to provide the five dots of the horizontal character line. The sixth dot position is always blanked. While the shift register is being emptied to display one scan line of a character, the corresponding scan line from the next character is being fetched from memory.

Six bits of the eight-bit wide memory are required to define any one of the 64 possible characters. The two additional bits are used to allow any characters to be displayed in inverse (black on light) or to be blinked on and off at a 2-Hz rate.

The horizontal raster generator runs at 19.8 kHz (above the range of audibility for most people) to avoid the annoying whistle common to raster-scan displays running at the TV-standard frequency of 15.750 kHz. The line and frame generator circuits follow standard raster-scan design practice by using an LC ringing circuit to achieve a fast retrace with low power dissipation. Special precautions were taken, however, to insure a linear display. For example, display centering, necessary because of production tolerances in the CRTs and yokes, is performed by sending a bias current through the yoke windings rather than by the more common practice of using adjustable ring magnets at the neck of the CRT. This causes all deflection to take place at the design center of the yoke, resulting in a better quality display.

Acknowledgments

The initial mechanical design of the 1611A was done by Don Bloyer before his move to Hewlett-

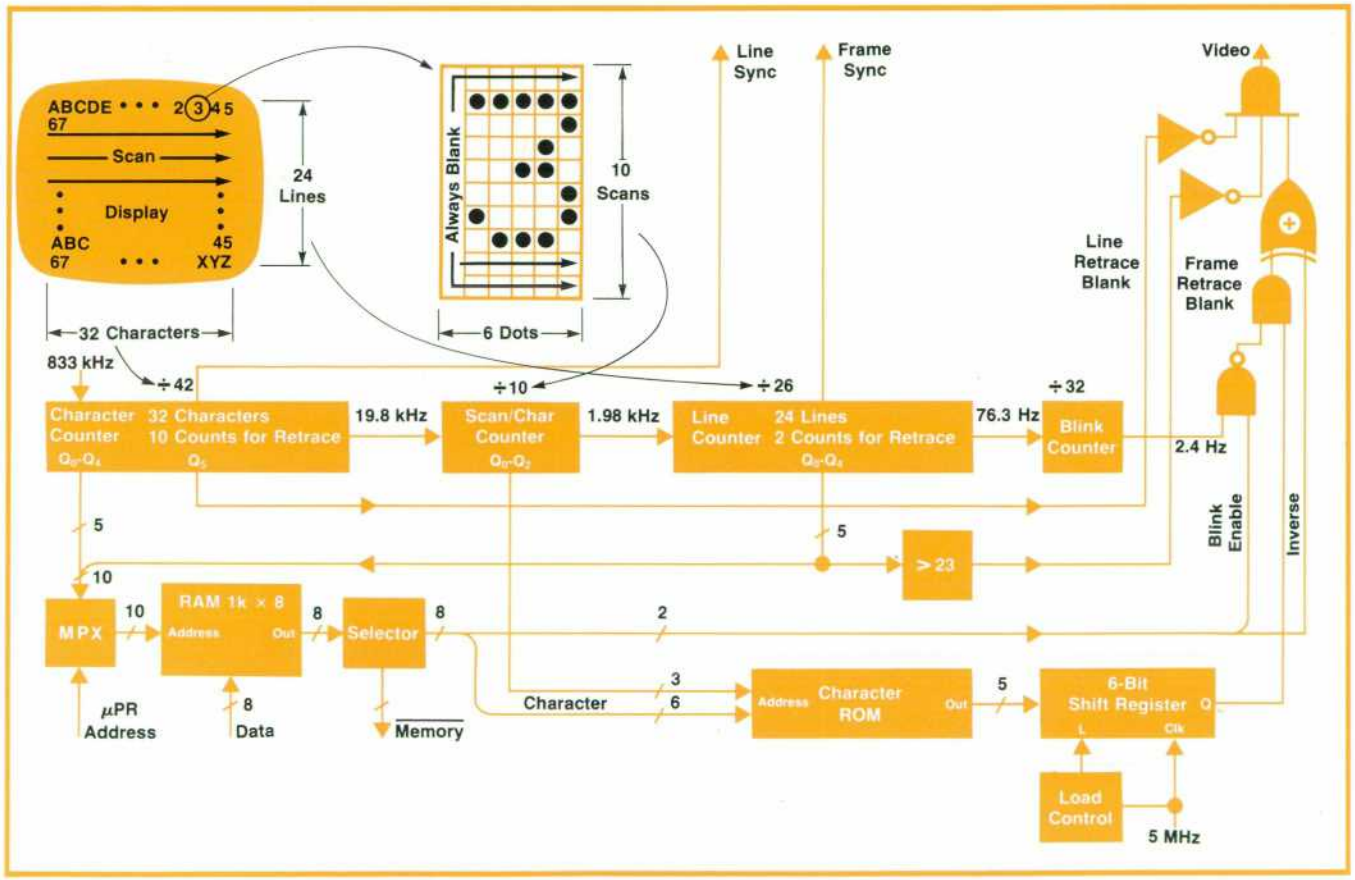


Fig. 10. *Simplified diagram of the display logic for Model 1611 Logic State Analyzer.*

Packard's Data Terminals Division. The design of the probing system was completed by Don Miller, while Roger Molnar did the product design for the mainframe and personality modules. The display and power supplies were designed by Dick Wolfrum. Tom Saponas wrote all of the software and designed the 8080 personality module. Special thanks are due Lori Allgood, Larry Koperski and Roger Molnar for smoothing the sometimes difficult transition from a laboratory design to a production instrument.

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Jeffrey H. Smith

After earning BSEE and MSEE degrees at Stanford University, Jeff Smith joined HP's Oscilloscope Division in Palo Alto (1963) and moved with the division to Colorado a year later. He has contributed to several units of the HP sampling oscilloscope family, was project leader for the Model 1815A Time Domain Reflectometer, and was responsible for four high-speed modules in the 1900-series Pulse Generators. He became involved in several investigative projects before undertaking the Model 1611A Logic State Analyzer. In his spare time, Jeff likes to ski, fish, and explore the Rocky Mountains in his 4-wheel-drive vehicle. He's married and has two small children.

SPECIFICATIONS

HP Model 1611A Logic State Analyzer

CONNECTION BETWEEN μP AND 1611A INPUT BUFFERS: one 40-pin dual in-line package connector with 30.5 cm (12 in) cable, one 40-pin male socket with 30.5 cm (12 in) or 7.6 cm (3 in) cable.
MEMORY DEPTH: 64 data transactions; 16 transactions are displayed at one time; roll keys permit viewing all 64 transactions.
TIME INTERVAL MEASUREMENT: Accuracy, 0.1% ±1 μs. Maximum time, $2^{24}-1$ μs (16.7 seconds).
EVENTS COUNT: $2^{24}-1$ events (16.7 million) max.

Personality Modules

Option 080

(Compatible with any microprocessor that meets the specifications of the Intel 8080A.)
CLOCK (ϕ_2 only)
REPETITION RATE: 300 kHz to 4 MHz.
WIDTH: 75 ns minimum for either high or low state.
THRESHOLD: 9 to 13 V, logic 1 (high): −1 to 0.8 V, logic 0 (low).
INPUT RESISTANCE: approx 12 kΩ.
INPUT CAPACITANCE: approx 25 pF with 30.5 cm (12 in) cable; approx 15 pF with 7.5 cm (3 in) cable.
DATA, ADDRESS, WAIT, READY, HLDA, INTE, SYNC
THRESHOLD: 3 V to 6 V, logic 1 (high); −1 to 0.8 V, logic 0 (low).
INPUT RESISTANCE: approx 1 MΩ.
INPUT CAPACITANCE: approx 25 pF with 30.5 cm (12 in) cable; approx 15 pF with 7.6 cm (3 in) cable.
SETUP AND HOLD TIMES (timing measured at 8 V level for leading edge of ϕ_2 and 1 V level for trailing edge):
Address and μP status on Data lines relative to leading edge of ϕ_2 at T_2, data relative to leading edge of ϕ_2 at T_3, and sync relative to trailing edge of ϕ_2 at T_1:
SETUP: 100 ns min.
HOLD: 25 ns min.
Ready relative to trailing edge of ϕ_2 at T_2:
SETUP: 80 ns min.
HOLD: 0 ns min.
READY OUTPUT: TTL open-collector-compatible output capable of sinking at least 8 mA when active.
OUTPUTS (Low <0.4 V into 50Ω and High >2.0 V into 50Ω, nominally 3.9 V into an open circuit, with all timing relative to leading edge of ϕ_2 in T_3 cycle):
TRIGGER: duration approx 75 ns (RZ format); delay approx 350 ns after ϕ_2 clock pulse that defines a valid trigger.
TRACE POINT (⎽⎺⎽): positive edge approx 350 ns after ϕ_2 clock that defines specific valid trigger to be displayed. If Delay is set such that trigger is not displayed, Trace Point output occurs approx 350 ns after ϕ_2 clock that defines valid trigger word immediately preceding first word displayed.
TRACE POINT (⎺⎽⎺): complement of Trace Point (⎽⎺⎽).

Option 068

(Compatible with any microprocessor that meets the specifications of the Motorola 6800.)
CLOCK AND DATA INPUTS
CLOCK RATE: 70 kHz to 1.4 MHz.
INPUT RESISTANCE: approx 1 MΩ for all inputs.
INPUT CAPACITANCE: approx 30 pF for D_0-D_7 inputs, approx 40 pF for all other inputs. Includes capacitance of 30.5 cm (12 in) connecting cable; approx 10 pF less with 7.6 cm (3 in) cable.
THRESHOLD: 2.4 V to 5.5 V, logic 1 (high); −0.8 V to 0.8 V, logic 0 (low).
SETUP TIME: D_0-D_7 must be present prior to falling edge of ϕ_2 clock for at least 110 ns. HALT must be present prior to leading edge of ϕ_2 clock for at least 250 ns. All other inputs must be present prior to falling edge of ϕ_2 clock for at least 250 ns.
HOLD TIME: HALT must be present after leading edge of ϕ_2 clock for at least 10 ns. All other inputs must be present after falling edge of ϕ_2 clock for at least 10 ns.
HALT OUTPUT: TTL open-collector-compatible output capable of sinking at least 8 mA when active.
OUTPUTS (Low <0.4 V into 50Ω, High >2.0 V into 50Ω, nominally 3.9 V into an open circuit):
TRIGGER OUTPUT: duration approx 75 ns in RZ format; delay approx 550 ns after active edge of ϕ_2 clock pulse that defines a valid trigger.
TRACE POINT (⎽⎺⎽): positive edge approx 550 ns after ϕ_2 clock pulse that defines specific valid trigger to be displayed. If delay is set such that trigger word is not displayed, Trace Point output occurs approx 500 ns after active edge of ϕ_2 clock that defines valid trigger immediately preceding first word displayed.
TRACE POINT (⎺⎽⎺): complement of Trace Point (⎽⎺⎽).

External Probe Inputs

RESISTANCE: approx 1 MΩ.
CAPACITANCE: approx 25 pF measured at probe tip.
THRESHOLD: 2.4 V to 5.5 V, logic 1 (high); −0.8 V to 0.8 V, logic 0 (low).
SETUP TIME: input must be present for at least 250 ns prior to falling edge of ϕ_2 clock.
HOLD TIME: input must be present for at least zero ns after falling edge of ϕ_2 clock.

General

LOGIC PROBE OUTPUT POWER: 5 V dc at 0.1 A max.
LINE POWER: 100, 120, 220, 240 V ac; −10% +5%; 48 to 440 Hz; 120 VA max.
DIMENSIONS: 425 mm W × 190 mm H × 572 mm D (16¾ × 7-7/16 × 22½ in).
WEIGHT: 15 kg (33 lbs).
PRICE IN U.S.A.: Model 1611A Logic State Analyzer (Option 068 or 080), $5000.
MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road
Colorado Springs, Colorado 80907 U.S.A.

Firmware for a Microprocessor Analyzer

By replacing hardware with firmware, the instrument designer can increase operator convenience and present data in a more meaningful form without increasing circuit complexity. Here is how this capability was applied to a logic state analyzer.

by Thomas A. Saponas

EASE OF OPERATION was the fundamental design criterion for the firmware in the Model 1611A Logic State Analyzer. The keyboard and display were to be kept as simple as possible despite the complexity of the measurements that the instrument is capable of making. Furthermore, instrument operation was to be optimized for the most often used modes of operation so the analyzer could be of service even to users who may not have acquired complete knowledge of all the instrument's capabilities.

The keyboard contains the primary controls for the instrument, replacing what would have been a bewildering array of knobs, switches and pushbuttons. It was essential to devise a keyboard layout that provided simplicity of use for the novice as well as convenience for the experienced user. Hence, the keys are grouped into four functional areas: TRACE SPECIFICATION, ENTRY, EXECUTE, and DISPLAY (see Fig. 1). Also, the keys most basic to instrument operation are in a darker shade to distinguish them as the primary keys of the instrument.

The TRACE SPECIFICATION keys select the measurement options that define the specific conditions of the "snapshot" of the data sequence to be captured and displayed. For example, if it is desired to trace program flow beginning at a specific address, the ADDRESS BUS= key in the TRIGGER section is pressed first, then the desired address is typed in using the keys in the ENTRY group. Data capture and display beginning

Fig. 1. *Keys are grouped into four functional areas on the keyboard of the Model 1611A Logic State Analyzer. The keys that are most basic to instrument operation are in a darker shade.*

at that address is initiated by pressing the TRACE key in the EXECUTE section.

Keyboard-Display Interaction

Whenever a key in the TRACE SPECIFICATION group is pressed, an inverse video field (black on white) is created on the display and a blinking cursor shows the position of the next digit to be entered (Fig. 2). When all of the allowed character positions are filled, the field is closed and the display reverts to normal video (white on black). It is not necessary to fill all the positions to close the field—opening another field with a TRACE SPECIFICATION key or initiating a measurement with an EXECUTE key will close a partially filled field. The closed field then has implied leading zeros (except fields specified by an EXT= key, which have binary information only with unspecified positions filled with X's, for don't care).

Twelve separate fields are available within the TRACE SPECIFICATION group for defining the measurement specifications. The majority of measurements are performed with only a few of these. When turned on, the instrument turns off all these options except the TRIGGER ADDRESS BUS= field, which is open. The off state means these options are in the appropriate default modes and are not displayed. A new field appears on the display whenever the corresponding key is pressed. If a field is no longer needed, it can be eliminated by opening it, entering a DON'T CARE, and closing it again.

An important part of the keyboard-display interaction is the provision for error messages in the case of illegitimate key sequences. For example, if a key in the ENTRY group is pressed when there is no open data field, the resulting message is simply: NO OPEN DATA FIELD. Or, if an attempt is made to enter other than binary data in an external data field, the message ILLEGAL KEY appears. There are eighteen separate error and warning messages—using English rather than numeric codes—to provide useful feedback on the status of the analyzer to the operator.

Automatic repeat functions for keys, a useful feature often found in CRT terminals, are applied sparingly in the logic state analyzer. In the case of the TRACE SPECIFICATION keys, repeated operation serves no useful function whatever. As for the ENTRY keys, the annoyance of having a key repeat unintentionally outweighs the advantages of repetition, since the longest data field is only eight characters wide, so no repeating keys are provided here. All of the EXECUTE keys, on the other hand, will start repeating at a rate of ten executions per second when held past an initial delay. Repetitive measurements are often desirable to visually monitor changes in data. The roll up and roll down keys in the DISPLAY group, used to scan through the analyzer's memory, have a similar repeating action, allowing either a one-line step or a continuous roll of the data through the display.

The 10/s repetition rate was chosen because it's about the highest rate permitting visual and manual response sufficient to stop the repetition at the desired point.

The freedom to implement these characteristics with no increase in circuit complexity or cost is another example of the power inherent in microprocessor-based systems.

Fig. 2. *When a TRACE SPECIFICATION key is pressed an inverse video field is created. The black underline in the white field blinks to show where the next character entered will be positioned. When the field is filled or closed by other means, the display automatically reverts to normal video.*

Display Format

The display format possibly contributes more to the effectiveness of the new logic state analyzer than does the ease of defining and performing a measurement. Monitoring any CPU, whether a microprocessor or a large computer, inherently results in the generation of vast amounts of data. Interpretation of all this data can be simplified in two ways. First is by being selective about the measurement to be performed so there is not so much data to be analyzed. The many new capabilities of Model 1611A offer substantial improvements in this area over the simple breakpoint and trace functions commonly found in most digital analysis tools. Second is the use of a mnemonic format that in itself further condenses the data.

Previous logic state analyzers presented the flow of data as a table of binary words. The mnemonics, on the other hand, are abbreviations of the functions to be performed by the microprocessor (e.g. CLA represents "clear the accumulator") so reading the flow of program execution is considerably easier with mnemonic than it is with binary words. The ROM supplied in the analyzer's personality module causes the display to show the mnemonic codes used by the manufacturer of the microprocessor being monitored, so the displayed data will be similar to the source assembly listing used to generate the code (Fig. 3). Even if a high-level language were used to generate code, a mnemonic translation is normally available for program debugging.

When operating in the mnemonic mode, all of the memory fetches required to describe an instruction

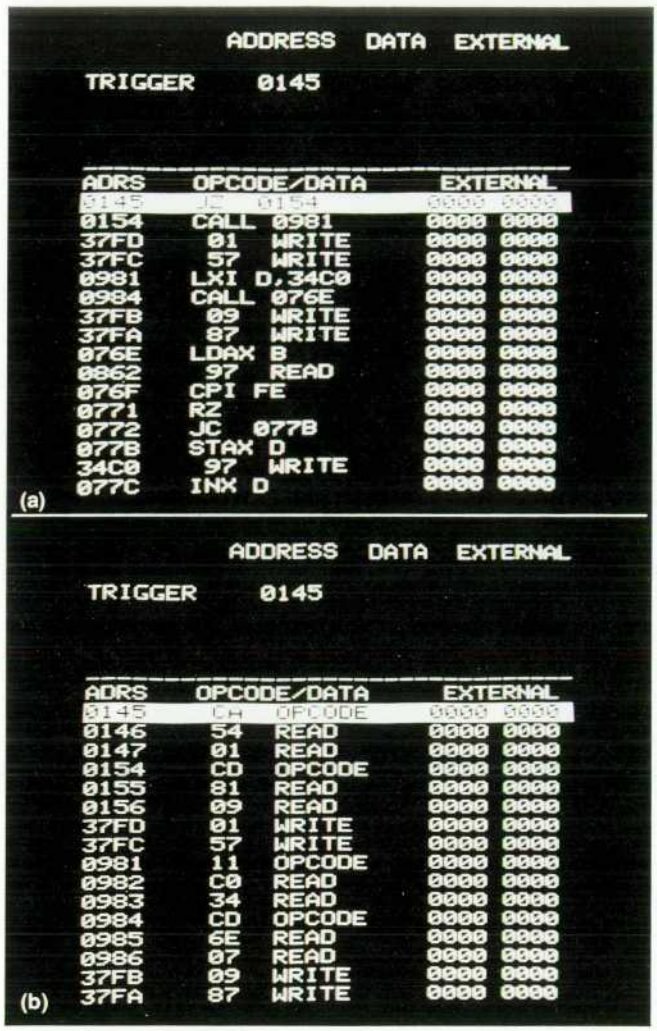


Fig. 3. *Display in the mnemonic mode (a) lists the operation in the assembly language of the microprocessor being tested. If an instruction causes additional data transfers, these are displayed indented. The same sequence listed in (a) is shown in the absolute format in (b) below.*

(normally one to three fetches) are stored in the analyzer's memory but are condensed into one line containing the mnemonic and the operand on the display. Then if the instruction causes additional transfer of data, these subsequent transactions are displayed indented on the following lines with a description of the type of transaction performed (Fig. 3). The analyzer also stores the status of the eight external lines and displays them in binary. These lines help find problems outside the microprocessor's address and data buses, and enable a detailed look at the system I/O, very often the part of the system that is most difficult to design and debug.

The stored data can also be displayed in absolute format where each line displayed represents one memory transaction and contains the address and data in hexadecimal or octal format, followed by a description of the type of transaction and the external data (Fig. 3). The change from one mode to the other is effected by the MNEMONIC/ABSOLUTE key, which only modifies the display and does not affect the data in the analyzer's memory. This is also true of the HEXADECIMAL/OCTAL switch.

Firmware Operation

Data acquisition is performed in dedicated hardware because the incoming data rate could be too high to be handled by the internal microprocessor. The other firmware tasks are control of the high-speed front end and the previously mentioned keyboard and display functions. Because of the relatively slow response time required for these functions, an interrupt-driven operating system is not used in the firmware. Instead, all important inputs simply are polled.

At power up, the internal memory is exercised and a checksum is performed on the ROM to verify that the internal processor system is functioning. A message indicating that the self check is completed is displayed on the screen, along with any error conditions that were found. All internal pointers and hardware are initialized and the unit then waits for inputs.

The flow chart in Fig. 4 shows that the firmware has two operating modes: measurement specification and measurement execution. As previously described, the measurement specification mode involves opening and closing data fields and the entry of numbers into those fields.

A basic function of the logic state analyzer is to supply output pulses in synchronism with the triggering condition. These pulses can be used by an oscilloscope or other instrument when tracking down hardware problems. It is therefore important that the high-speed memories used as arithmetic comparators reflect the current condition displayed on screen. Consequently, these memories are reloaded any time a keyboard stroke modifies the trigger conditions.

In the measurement execution mode, the high-speed input section is initialized for the run type to be performed and then the run starts. The processor monitors the status of the front end and describes the progress of the measurement by displaying appropriate messages, such as WAITING FOR TRIGGER, or TRIGGER OCCURRENCES =15 (when the trigger conditions were specified, for example, to start data capture on the 18th trigger occurrence). The keyboard continues to be read in this mode so the operator can abort the measurement at any time by pressing the appropriate key. Normally, display of the data in the high-speed memory does not start until the run is completed. Count and time measurements, however, are continuously updated while the measurement is in progress.

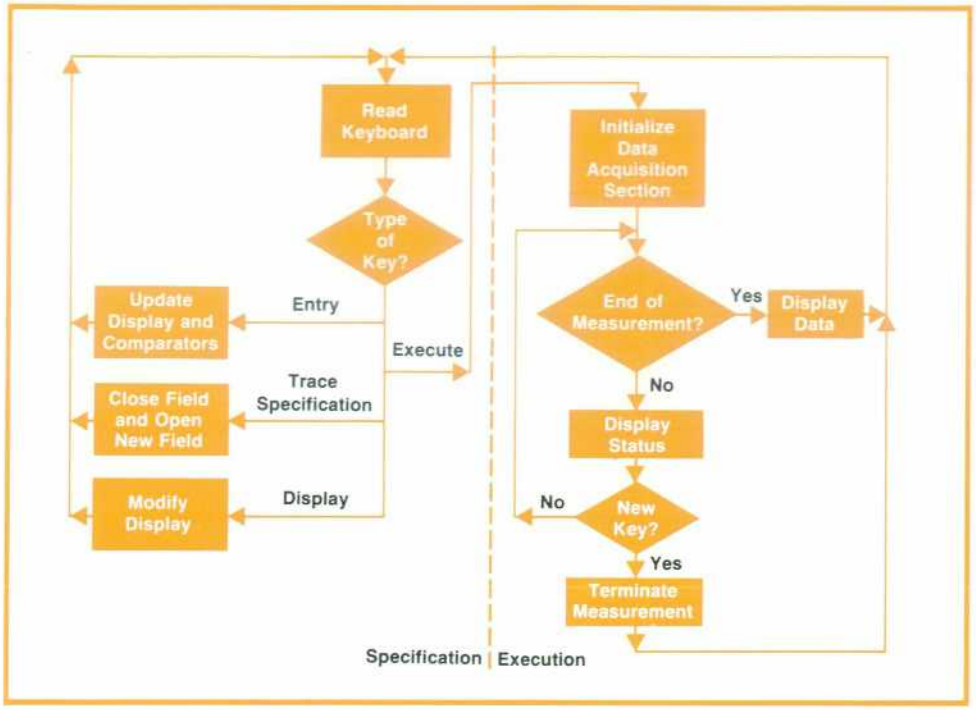


Fig. 4. *Flow chart of firmware operation.*

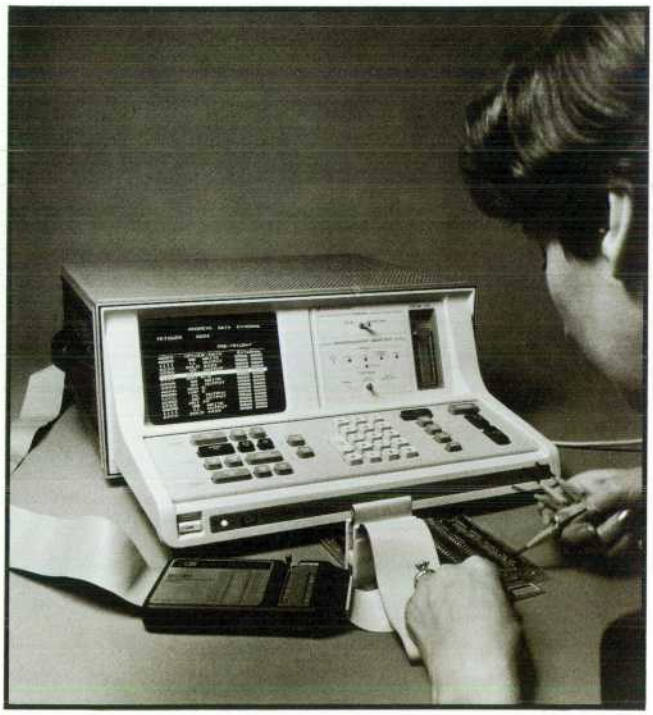
The inverse assembly process to obtain the mnemonic listing is performed a line at a time after the run is completed. The listing is stored in a slow RAM for repetitive readout. This is done only for the 16 lines on display to reduce the amount of slow RAM required. When the display is rolled in either direction, the new data is converted and stored.

Conclusion

The use of a microprocessor has brought numerous improvements to a logic state analyzer. Simplicity of operation and convenience were increased despite greater capability and complexity. The data is displayed in more meaningful and varied formats yet, by replacing hardware with firmware, the actual amount of circuitry was reduced.

Acknowledgments

The keyboard layout and terminology was largely the work of Jim Williams. Many useful inputs about the keyboard-display interaction were provided by Dick Cochran, Bruce Farley, and Bill Farnbach.



Thomas A. Saponas

A native of Colorado Springs, Tom Saponas obtained a BS degree in computer science/EE and an MSEE degree from the University of Colorado (1972). He then joined HP's Automatic Measurements Division in Palo Alto to work on digital systems. As the Colorado Springs Division became involved in logic state analyzers, he transferred there in 1974 to work on the Model 1607A and then the Model 1611A. Tom maintains autos as a hobby, mostly sports cars, and also enjoys hiking, camping, and playing bridge. He and his wife designed their own home and had it built in the community of Black Forest just in time to welcome their first born.

A Versatile, Semiautomatic Fetal Monitor for Non-Technical Users

A new monitoring instrument detects the heart beat of an unborn child by any one of four techniques. It does not require technically trained people to operate it, so the benefits of fetal monitoring now become available to a wider range of hospitals.

by Erich Courtin, Walter Ruchay, Peter Salfeld, and Heinz Sommer

CONTINUOUS MONITORING of the heart rate of an unborn child has proved itself to be a valuable tool for modern obstetrics. By providing an early indication of fetal distress, a fetal heart-rate monitor enables more effective management of the patient. Hospitals report that the use of fetal heart-rate monitoring has led to substantial reductions in infant mortality and morbidity rates.[1,2,3]

As with other modern medical techniques, fetal monitoring was initially applied by research-oriented practitioners who had some familiarity with instrumentation and who could manage the various sensitivity controls and other adjustments that the equipment needed for coping with the great variety of signal characteristics that were met in day-to-day practice.

Now that the benefits of fetal monitoring have been well proven, and its use in general practice is growing, a need exists for instruments that can function in a non-research-oriented environment, instruments that require little more than the turning on of a power switch to operate. These would allow the user to concentrate on patient care rather than instrument operation. This was the design goal for the Hewlett-Packard Model 8030A Cardiotocograph (Fig. 1).*

Operating Simplicity

Four different techniques for monitoring the fetal heart rate have been developed and proved useful (see box, next page). The new Model 8030A makes any combination of the four available for each installation by providing all of the circuits unique to a particular method on a single circuit card. The mainframe is arranged so the capability of measuring by any method

*Cardiotocograph: derived from the Greek words kardia (heart), tokos (childbirth) and graphos (something written).

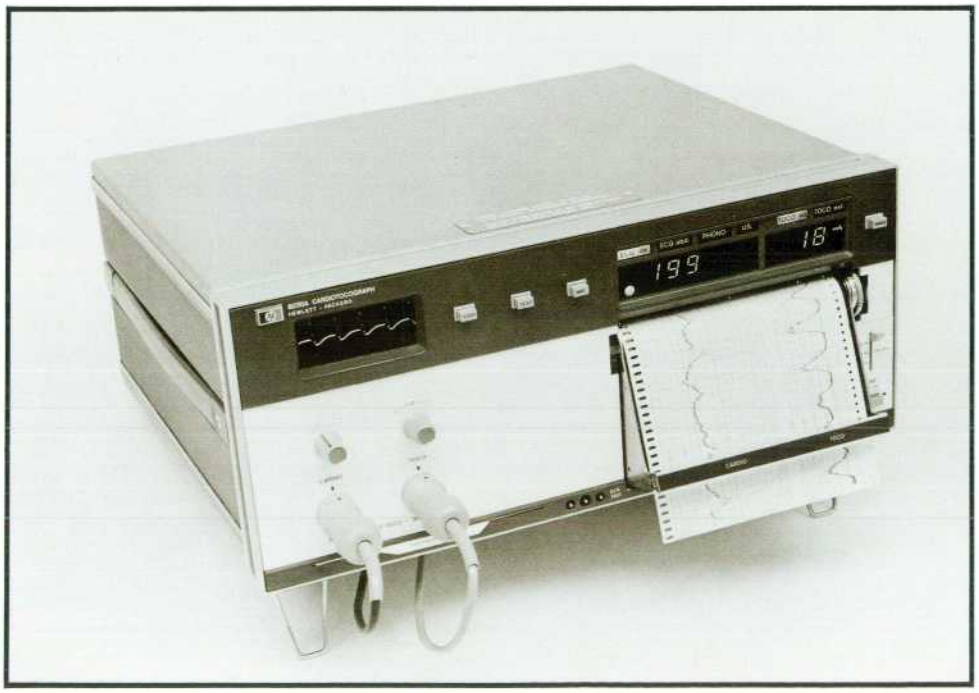


Fig. 1. *Model 8030A Cardiotocograph monitors fetal heart rate and plots it on its built-in strip-chart recorder along with a plot of labor activity. The instrument can monitor fetal heart rate by any one of four techniques and its design combines this versatility with operating simplicity and compactness.*

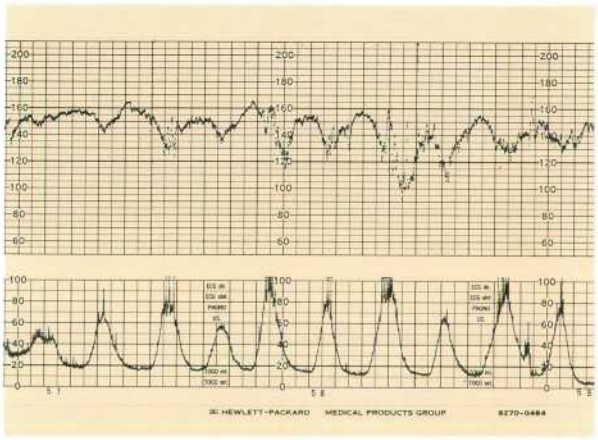
Fetal Monitoring—Towards Improved Management of Pregnancy and Delivery

Fetal monitoring systems alert doctors to threatening prenatal situations long before they can be detected by other means. As a result, corrective action can be taken at the appropriate time, reducing the chances of a depressed infant being born.

These systems monitor the unborn baby's heart rate and record its reactions to labor contractions and other stresses. The physician is provided two traces on a strip chart recording, one plotting the fetal heart rate and the other the mother's labor activity. The manner in which fetal heart rate varies in response to stimuli like labor contractions provides the doctor with the information needed to judge fetal well-being.

The first electronic fetal heart-rate monitor was developed in 1961 by Dr. Edward H. Hon, then of Yale University. The system used a tiny bipolar electrode that was attached to the infant's scalp as soon as the membranes broke. This direct monitoring technique gives a well-defined ECG signal, and because of that it is highly useful, but only in the later stages of delivery.

Potentially critical cases need to be recognized sooner, so many researchers have continued to search for ways to measure fetal heart rate without direct contact. In the early sixties, Dr. K. Hammacher, then of Dusseldorf University, Germany, developed a monitor that derived fetal heart rate from the sounds generated by the fetal heart. The first commercially-available fetal monitor, HP Model 8020A Cardiotocograph introduced in 1968, was based on this technique.



The advantages of this type of heart-rate monitoring are that it is external, passive, and can be used beginning at about the sixth month of pregnancy. However, the technique is sensitive to speech, the rustling of bedclothes, and other noises. The technique also may not prove satisfactory for an obese patient.

In 1971 Hewlett-Packard introduced a second approach to external fetal heart monitoring (Model 8021A). This technique uses ultrasound to sense the movement of the fetal heart valves using a transducer strapped to the mother's abdomen. It is effective with the patient in any position and unaffected by environmental noise. This system does, however, require that the beam be confined to a narrow cone to maintain adequate signal-to-noise ratios. Operation can be affected by positioning error or patient movement. Another version generates a broader ultrasonic beam that responds to the movement of the heart walls. Although this version is less sensitive to positioning errors, and is thus more suitable for long-term monitoring, it does not produce as sharply defined a pulse as the narrowbeam transducer so it is not adaptable to sensing beat-to-beat changes in fetal heart rate. Its major use is in screening patients.

Research directed at developing a technique for obtaining the fetal ECG through external electrodes attached to the mother's abdomen was undertaken because the abdominal ECG technique, which is passive, needs only lightweight electrodes that cause little patient discomfort in long term monitoring and that allow the patient to move and lie in any position. Past efforts required complex equipment and highly skilled operators but a recently developed abdominal ECG (AECG) technique, available with the HP Model 8030A Cardiotocograph, can be used by hospital personnel who do not have any training in electronics.

Clinical trials have shown that the AECG technique is effective in the great majority of cases except where patient restlessness develops interfering muscle potential, or in rare cases where the amniotic fluid fails to provide adequate electrical coupling from fetus to mother. The patient cable for the AECG technique has been designed to accommodate electrodes for direct monitoring. Thus, in the later stages of delivery when the membranes rupture, the physician can switch instantly to direct monitoring.

All of these monitoring techniques are available with the new Model 8030A Cardiotocograph, described in the accompanying article.

can be given the instrument simply by plugging in the appropriate card (Fig. 2).

This plug-in approach does not complicate instrument operation, however. Operating simplicity was achieved for the Model 8030A by providing only *one* connector on the front panel for the heart-rate transducer cable and *no* mode selector switch. When a transducer cable is connected to the instrument, the circuits appropriate to the transducer are automatically switched in. If by any chance the appropriate circuits have not been installed, a front-panel INOP indicator turns on.

A second front-panel connector is provided for the labor-activity transducer. The cable connectors are color-coded to show which socket a cable should plug into, and the pin arrangements differ so it is not possible to plug a transducer cable into the wrong socket.

Automatic Operation

Once transducers are connected and placed on the patient properly, the instrument automatically selects the optimum sensitivity range and displays fetal heart rate and labor activity on its digital display. A small indicator in the lower left corner of the display blinks and a loudspeaker beeps in synchronism with the detected fetal heart beat to provide visual and aural confirmation that the instrument is working. The dual-trace recorder plots heart rate and labor activity simultaneously, providing the record of the relationship between fetal heart rate and labor activ-

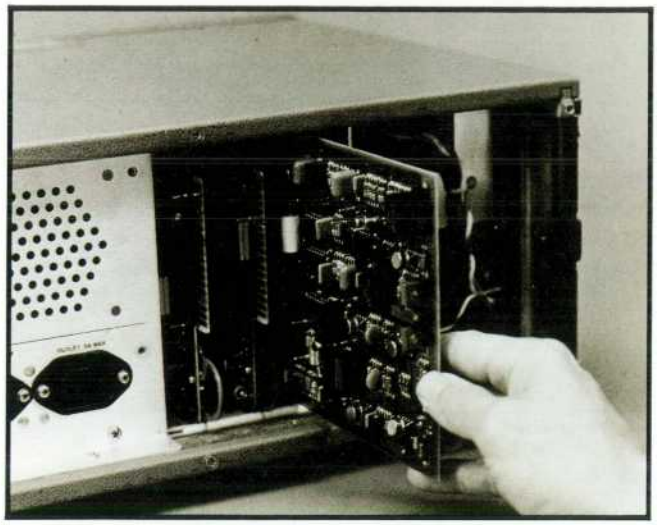


Fig. 2. *Adding another monitoring technique to the Model 8030A Cardiotocograph is simply a matter of inserting a circuit card and then using the corresponding transducer. The instrument automatically makes the necessary circuit connections for whatever transducer is in use.*

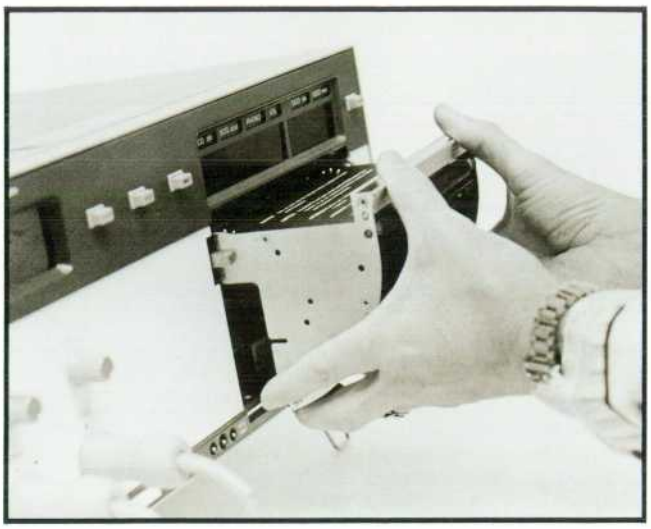


Fig. 3. *Swinging the paper table up to the horizontal position allows the paper magazine to be withdrawn for easy loading.*

ity that the physician needs for assessing fetal well-being.

An indication of how well the heart rate transducer is positioned is provided by a built-in CRT display of the fetal heart signal, which also shows the presence of muscle artifact or powerline interference. Digital storage provides a non-fading display of the most recent 1.5 seconds of signal. Pressing the STOP button "freezes" the trace for detailed examination of transients.

CRT operation is automatic. Brightness is adjusted for ambient lighting conditions by a light sensor behind the translucent Hewlett-Packard emblem and full-scale deflection is maintained by automatic level-control circuits.

The instrument's recorder uses thermal writing and thus avoids the possibility of running out of ink. Each "stylus" is a thick-film resistor similar to those used in HP calculator printers.[4] "Pen lift" is simply a matter of turning the stylus off, thereby eliminating the clatter of a mechanical pen lift. To make operation quieter, contactless position feedback is provided by a capacitive transducer on the galvanometer shaft.[5] This "touchless" feedback also enhances reliability by eliminating mechanical parts that could wear out. The galvanometer, which needs a frequency response of only 3 Hz, is positioned by a servo motor through a silent step-down belt drive. Recording sensitivity is 20 beats-per-minute/cm, giving a basic resolution of 1 bpm for seeing small changes in heart rate.

The paper is advanced by a direct-drive stepping motor, eliminating the usual gear train. Paper speed is changed simply by switching to a different motor drive frequency, rather than by shifting gears. The paper magazine was designed to make loading the chart paper extremely easy (Fig. 3).

To eliminate the bother of unnecessary service calls, self-check capabilities are included. Pressing the TEST pushbutton causes the instrument to display a heart rate of 200 and to add 50 to the labor activity indicator, giving a check on the operation of the displays and recorder. A test socket (ECG TEST) on the front panel supplies a simulated ECG to the electrode connector on the ECG cable to check out the cable and the input amplifiers, as well as the rest of the instrument.

Inside the Instrument

Plugging a transducer cable into the instrument automatically connects a resistor in the cable in series with a voltage source and a resistor within the instrument. Each type of transducer cable has a different value resistor so the voltage drop across the internal resistor is indicative of the type of transducer connected. Comparator circuits monitor this voltage, switch in the appropriate circuits, and turn on the corresponding front-panel mode indicator. The instrument thus automatically selects the right circuits whenever a transducer cable is plugged in.

The labor-activity transducers are pressure transducers that drive circuits for obtaining an electrical indication of pressure by conventional means, and need not be discussed further except to note that a recorder positioning control is provided for this channel. This was done because the baseline is affected by the static pressure on the transducer that results from tension on the belt holding the transducer in place. The control permits the operator to position the baseline on the zero-level line of the recording chart.

A Peak Pulse Detector

The waveforms obtained by the various fetal-heart-rate monitoring circuits described in the accompanying article very often do not have single peaks easily defined as heart beats, but may have complex waveshapes with several closely-grouped peaks at each heart beat (Fig. 1). The circuits must identify which of these peaks is the highest and, for the benefit of the heart-rate measuring circuits, exactly when the maximum value occurs.

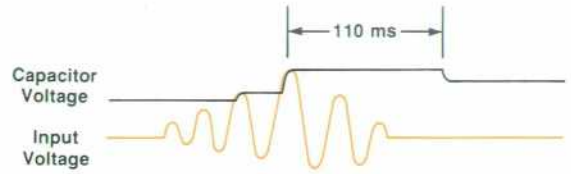


Fig. 1

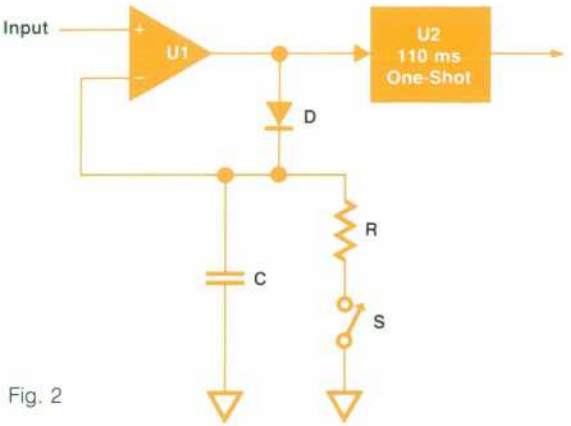


Fig. 2

The circuit shown in Fig. 2 does this by storing the maximum level of each peak for 110 ms or until a higher peak occurs, whichever occurs first. A heart beat is indicated only when a maximum is held for 110 ms.

Referring to the diagram in Fig. 2, a positive-going slope on the waveform causes U1 to act as a voltage follower, charging capacitor C to the same voltage as the input. When the input waveform reverses slope and starts negative, the charge retained on capacitor C back-biases diode D, decoupling the negative feedback loop around U1. The output of U1 then quickly swings to its negative saturation level. This quick drop triggers the one-shot multivibrator U2, starting the 110-ms interval.

If within the next 110 ms a higher input peak occurs, capacitor C charges to the higher value and the rise in voltage resets U2. When the waveform reverses slope again, the negative transition at the output of U1 triggers one-shot U2 once more, restarting the 110-ms interval.

If no higher pulse occurs within 110 ms, U2 returns to the set state at the end of the 110-ms interval. This transition generates a pulse for the fetal-heart-rate measuring circuits. It also closes switch S, discharging capacitor C for the next cycle.

The rate of discharge of capacitor C was made about 9 dB per second, found to be the best compromise. Too fast a discharge would make the circuit sensitive to noise peaks that could result in the generation of erroneous trigger pulses. On the other hand, if the discharge rate were too slow, a change in fetal-heart-beat amplitude could cause some beats to be missed.

In this way, a pulse is generated only in response to the highest peak of a group, and this pulse occurs precisely 110 ms after the highest peak reaches its maximum value where the slope changes from positive to negative. The 110-ms delay is of no consequence in the measurement of heart rate but the beat-to-beat timing is important, and this is readily established by this circuit.

Heinz Sommer

The basic function of any of the plug-in circuits selected for fetal heart-rate monitoring is to isolate the signal representing the fetal heart rate from other interfering signals. Mainframe circuits measure the period between beats, and the reciprocal of the period, which is frequency, is then presented on the front-panel display as fetal heart rate and converted to an analog voltage to drive the recorder. Measuring the beat-to-beat period and converting the measurement to heart rate enables the system to respond instantly to any changes in heart rate.

The direct ECG (DECG) method, which obtains a clearly defined fetal ECG from miniature electrodes clipped to the fetal scalp after the membranes rupture, involves straightforward amplification to obtain a waveform for driving the heart-rate measuring circuits. Unlike conventional ECG machines, however, the DECG circuits include a bandpass filter centered on the spectrum of a typical fetal ECG. This reduces the amplitude of any noise that may be mixed in with the signal. Also included is a polarity recognition circuit that controls a signal inverter so the heart-rate measuring circuits function regardless of the input signal polarity. Variations in signal level are accommodated by a peak detection circuit (see box above).

Abdominal ECG System

The abdominal ECG (AECG) system is more involved because of the relatively low level of the fetal ECG—as low as 10μV peak—when sensed through electrodes placed on the mother's abdomen, and the relatively high level of interfering signals and the mother's own ECG, which may be 100 times larger (Fig. 4).

In the AECG circuits, common-mode signals are suppressed by the input amplifier, a low-noise differential amplifier that has a wide dynamic range. A sizable normal-mode signal remains, however, a circumstance to be expected whenever electrodes spaced a few inches apart are attached to the human body in a hospital environment.

Powerline hum contributes by far the most to the

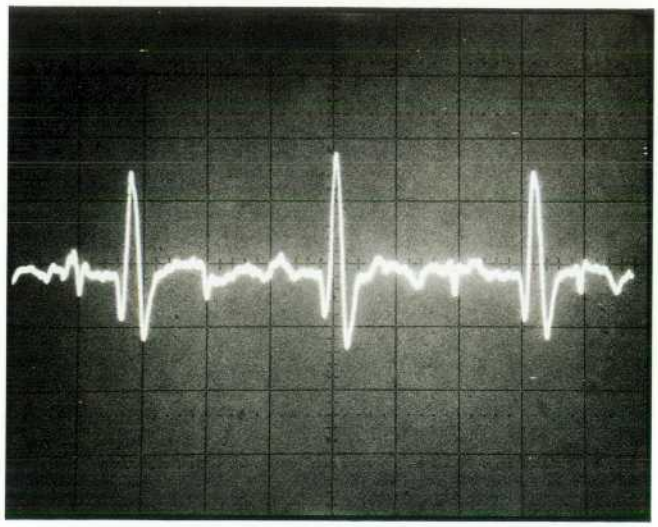


Fig. 4. *The fetal ECG (small negative peaks) is mixed with the maternal ECG (large peaks) and other interference when sensed by abdominal electrodes. The AECG circuits extract the fetal ECG from the composite signal.*

normal-mode interfering signal. This is suppressed by a notch filter following the input amplifier.

The signal path then splits into two channels: the maternal ECG channel, hereafter referred to as the M channel, and the fetal or F channel (Fig. 5). Since the frequency spectrum of the fetal ECG differs somewhat from the maternal ECG, some initial signal separation is achieved by using the appropriate bandpass filtering in each channel. Polarity recognition circuits in each channel accommodate signals of either polarity.

After filtering, the M signal is assured of being the largest signal component in the M channel, so it can be detected on the basis of peak amplitude. It is used to generate a blanking pulse for use in the F channel and in the pulse-insertion logic circuits.

The F channel has a 30-ms pulse generator that is triggered by the fetal ECG. It is inhibited, however, by the blanking pulse from the M channel so it will not generate a pulse in response to the maternal ECG signal feeding through to the F channel.

The pulse train generated in the F channel is fed to logic circuits. These determine the rate at which F channel pulses occur and if the timing indicates that there should be an F pulse at a time when one is blanked or missing, a pulse is inserted into the F channel output pulse stream. The logic circuits will *not* insert two pulses in a row, however, so there is no danger that the instrument will continue to output normal pulses when no fetal ECG is present.

The logic circuits also keep track of the maternal heart rate. If the M and F channels have exactly the same rate, they inhibit the F channel output during the maternal P wave (the P wave is a low-amplitude pulse that precedes by several milliseconds the large amplitude pulse, or QRS complex, of the maternal ECG). This precaution was taken because otherwise it could be possible that when no fetal ECG is detected, the F channel would respond to the maternal P wave and generate a train of pseudo-F pulses.

Detection by Ultrasound

The ultrasound system uses the Doppler shifts in frequency caused by movement of the heart walls or valves. The transducer's transmitting crystal radiates a 2.1-MHz CW acoustic wave into the body at a low-level (<10 mW/cm^2). The receiving crystal responds to the acoustic waves reflected from soft-tissue interfaces within the body. Filters extract the Doppler-shifted frequencies, rectify the signal and use the resulting waveform for the heart-rate monitoring circuits.

A block diagram is shown in Fig. 6. The transmitted signal that leaks into the receiving path serves as a local-oscillator signal for the mixing diodes in the demodulator. The output of the demodulator is dc except in the presence of a Doppler-shifted frequency,

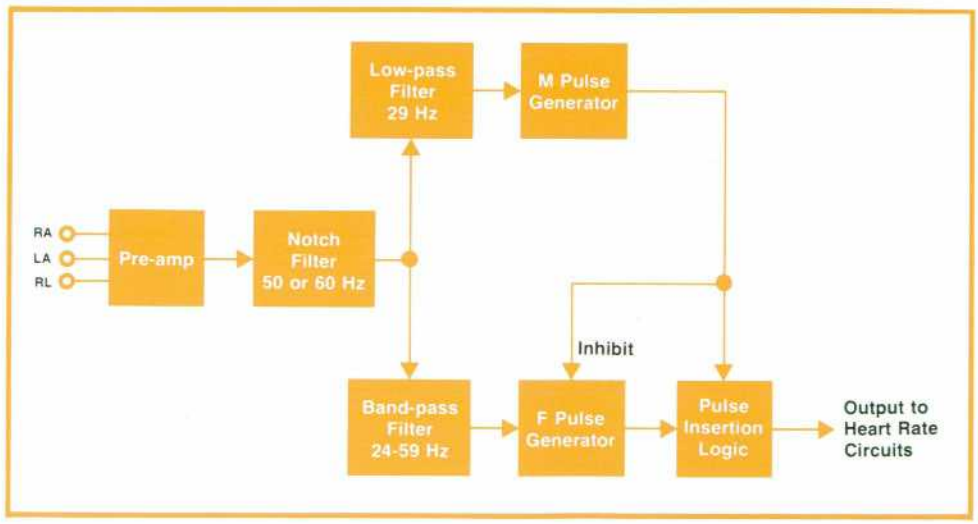


Fig. 5. *Simplified block diagram of the AECG circuits. The basic scheme is to blank the F channel during a maternal ECG beat so the maternal ECG will not generate an F pulse. If blanking occurs at a time when an F pulse would have occurred, the logic circuits insert a pulse into the output stream.*

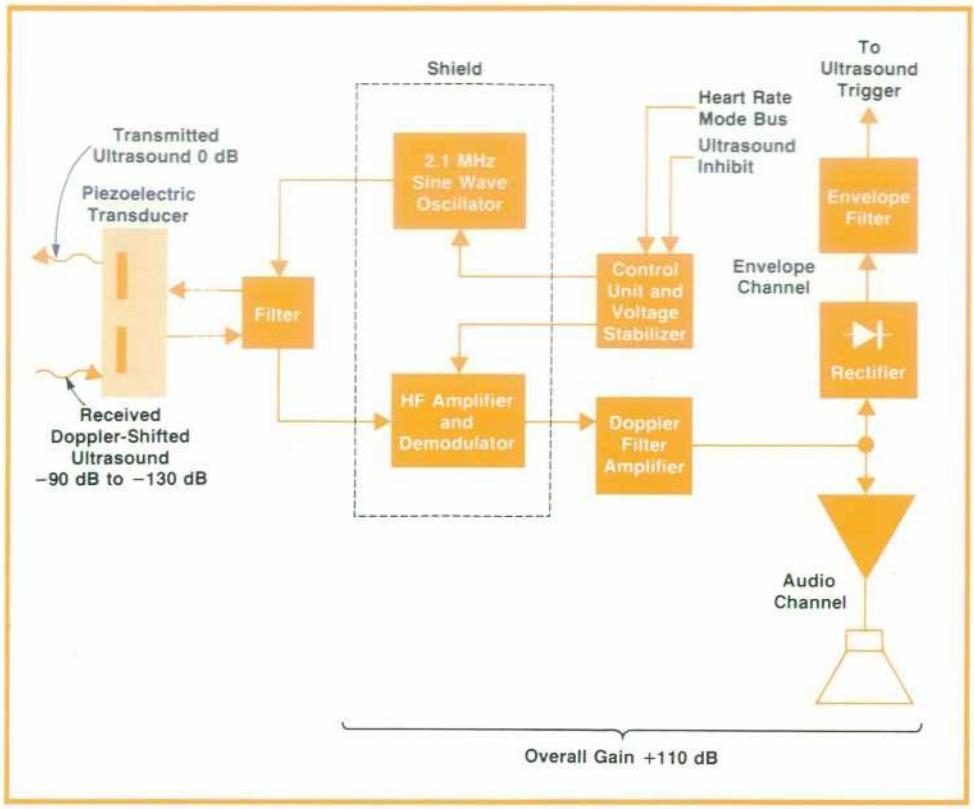


Fig. 6. *Simplified block diagram of the ultrasound circuit.*

in which case the output is the beat-frequency difference between the transmitted and received signals.

Bandpass filters extract the difference frequency resulting from heart movements and the result is rectified to obtain an envelope corresponding to the heart movement. This waveform is sent to the heart-rate circuits. The difference frequency is also supplied to the loudspeaker to give an audible indication of the occurrence of each heart beat.

The reflected signal is some 90 to 130 dB lower in amplitude than the transmitted signal. The high overall gain in the receiving channel (+110 dB) requires special measures to minimize the effects of interference. One measure used is a low-noise, low-distortion oscillator for the transmitter (amplitude noise: −120 dB). This reduces interference caused by oscillator harmonics beating with radio and TV signals. Other measures involve filters in the transducer connector for attenuating high-intensity, high-frequency radiation that could drive the amplifiers into a nonlinear operating region. The high-frequency section of the circuits is surrounded by both magnetic and electrical shields.

Actually, two ultrasound plug-in circuit boards were designed. One processes signals that have been Doppler-shifted by the heart walls. A bandpass filter centered on 265 Hz isolates the Doppler frequencies resulting from movement of the heart walls. The array transducer used with this circuit gives a broad ultrasonic beam that does not require careful positioning to obtain a strong doppler return from the relatively large heart walls.

The demodulated pulses from the heart walls, however, have relatively slow rise time. Because of the resulting impreciseness of the pulse timing, the beat-to-beat periods of these pulses are averaged over a period of about three beats to obtain a satisfactory fetal heart-rate tracing. Fine fluctuations in the actual heart rate are averaged out so this method is useful mostly for initial screening of patients to identify those that are potentially high risk.

The other ultrasound circuit board is designed for use with a highly directive transducer that responds to the fast movements of the heart valves, using a Doppler filter centered on 500 Hz. This system indicates beat-to-beat changes in heart rate and is therefore useful for critical cases. The transducer has to be carefully positioned, however, and movement of the fetus or the mother may necessitate frequent repositioning.

Phonocardiogram

The PHONO circuit board works with a piezoelectric transducer (contact microphone) placed on the mother's abdomen where it senses the sounds generated by the closing of the fetal heart valves. The transducer signal is bandpass filtered (70 to 100 Hz) to suppress other sounds picked up by the transducer.

The primary problem with using the phono signal for fetal heart rate monitoring is that more than one

heart sound may be detected per beat, depending on the transducer position. The circuits must therefore decide whether they are sensing one or two heart sounds per beat.

In HP's first Cardiotocograph (Model 8020A, 1968), rather complicated (and expensive) logic circuits examined the sound-to-sound intervals and decided whether one or two heart sounds were being sensed per beat. In the new Model 8030A, a detected heart sound triggers a one-shot multivibrator that inhibits succeeding heart sounds from reaching the following circuits for the duration of the one-shot. The circuit must be able to operate over a 4-to-1 range (50 to 210 beats/minute, or 1.2 to 0.285 seconds per period). This necessitated designing in the ability to adjust the one-shot on time to the heart rate. If the time between two triggers is less than 400 ms, the duration of the blanking pulse is 273 ms. If it is more than 400 ms, then the blanking pulse is extended to 346 ms.

Non-Fade Display

A shift register is used for storing the most recent 1.5 seconds of ECG signal for non-fade presentation on the CRT. The analog ECG signal is sampled every 3 ms and converted to an 8-bit word by an analog-to-digital converter, then fed into the shift register. At the same time, the oldest value is dropped off the last stage of the register.

Between samples, the shift register is put into the recirculating mode and all 512 stored values are read out sequentially in less than 3 ms and converted to an analog signal for display on the CRT. If the CRT horizontal deflection is timed to start in synchronism with the loading of a new sample into the shift register, the ECG waveform moves from right to left across the screen as though it were being written by a strip-chart recorder. If the start of the deflection ramp is advanced by one clock period each time, the waveform appears to stand still while a blanking bar moves across the screen, writing new data. The choice of display mode is made by an internal switch.

Pressing the front-panel STOP pushbutton prevents the input of new data into the shift register so the stored waveform can be retained for longer study.

Remote Monitoring

A subset of the cardiotocograph's capabilities has been configured into a cardiotocograph repeater (Model 8032A). This instrument (Fig. 7) has the same type recorder and digital display as the Model 8030A Cardiotocograph. It accepts the analog fetal-heart-rate and labor activity signals from an 8030A and reproduces them on its recorder. At the same time, its builtin voltmeter circuits display the signal levels. It can thus reproduce an 8030A's recording and digital readout at a remote location, such as at a nurses' station or in a doctor's office.

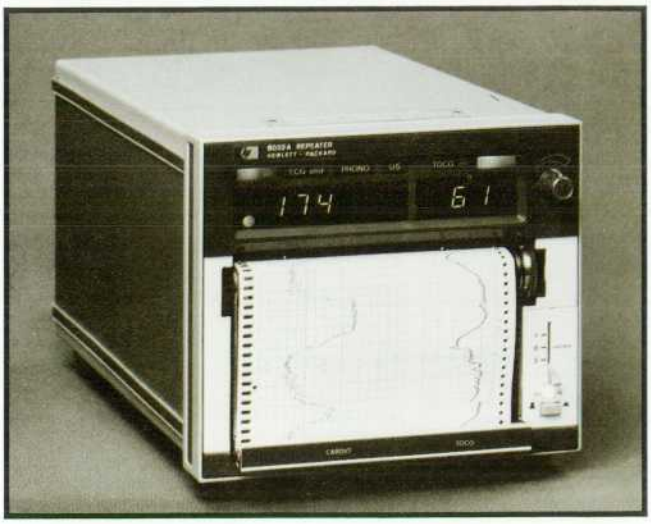


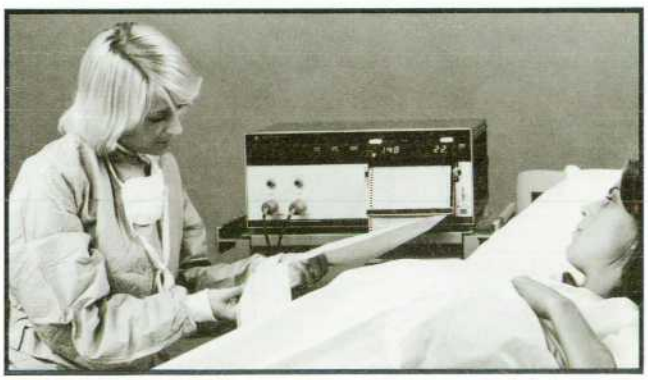
Fig. 7. *Model 8032A Repeater reproduces cardiograms recorded at bedside simultaneously at a remote location.*

The repeater also has indicators to show the monitoring techniques being used. This information is carried on two lines (one for heart rate and one for labor activity) that indicate the monitoring modes by dc voltage levels. Another line carries audio for the loudspeaker and one more line carries pulses for the "acceptance" lamp that flashes in synchronism with each detected fetal heart beat.

The repeater allows the obstetrical staff to study developments and discuss them away from the bedside, and it enables the staff to be constantly informed of a patient's progress when they can't stay with her all the time. It is also useful as a teaching aid because significant symptoms can be described to the nursing staff as they occur and without disturbing the patient.

Acknowledgments

Hilmar Spieth designed the ultrasound system, Hanno Ix the recorder, and Hans Peter Graf the digital readout circuits. The logic circuits were designed by Gerhard Weber. Mechanical design was by Rudiger Plessner, Eberhard Mayer and Ernst Heizmann and industrial design was by Dietrich Rogler.



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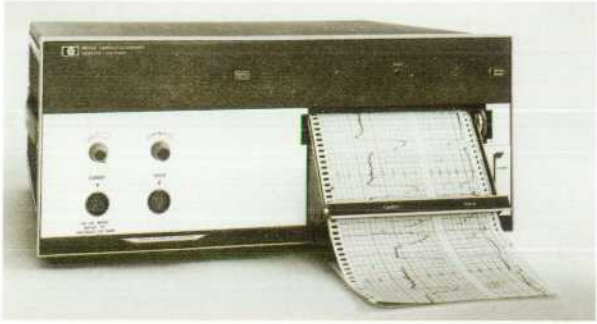
An Elemental Cardiotocograph

Where all the versatility of the Model 8030A Cardiotocograph is not needed, and where the information provided by the strip-chart recording by itself is sufficient, Model 8031A may fulfill a hospital's needs at lower cost. This instrument has the same ultrasound and direct ECG processing circuits as Model 8030A but omits the CRT and digital displays. It does have a loudspeaker and an "acceptance" lamp that flashes in synchronism with the fetal heart beat, providing aural and visual indications that the fetal heart beat is being detected.

The primary application of this instrument would be for dedicated antepartum monitoring, such as contraction stress testing (Oxytocin Challenge Test).

In addition to monitoring the fetal ECG directly or by the ultrasound method, both of which are standard, Model 8031A can also be configured to monitor by the phono (heart sound) technique. Monitoring labor activity by an external transducer is also standard. Monitoring internally by means of a catheter and pressure transducer is optionally available.

Model 8031A has the same automatic operating features as Model 8030A, including automatic selection of the appropriate circuits according to the transducer cable selected for use. The only controls are for loudspeaker volume, labor-channel zeroing, and recorder chart speed.



Erich Courtin

A graduate (diplom Ingenieur) of the University of Karlsruhe, Germany, Erich Courtin joined HP in 1968, working initially on the Model 8026A Ultrasound Monitor and then becoming project leader for the 15180A Ultrasound Transducer/Preamplifier. In 1972 he became section leader responsible for the development of the 8021A and 8030A Cardiotocographs. For relaxation, Erich plays table tennis or the violin. He and his wife have two children, 5 and 7.

Peter Salfeld

Peter Salfeld was involved six years in photometry for clinical chemistry before joining HP in 1972 to work on the abdominal ECG system and the isolated input amplifier. He's a graduate (Ingenieur Graduate) of Wolfenbüttel Engineering School, Germany. Peter spends much of his free time outdoors, sailing his kayak, backpacking, or on cross-country ski tours that may go for as long as three days. He and his wife have one child, 5.

Heinz Sommer

Heinz Sommer joined HP in 1967 upon getting his degree (Ing. Grad.) from the Staatliche Ingenieurschule in Duisberg. Initially he worked on acoustic instruments, subsequently becaming project leader for a sound-level meter. He transferred to the medical section in 1971 and was project leader for the Model 8021A Cardiotocograph before becoming project leader for the 8030A. Heinz enjoys sailing both on the water in his catamaran or in the air with a glider. He's married, but no children.

Walter Ruchay

Project leader for the abdominal ECG circuits, Walter Ruchay previously worked on acoustic instrumentation at HP, contributing to the 8052A Impulse Sound Level Meter and the 8055A Filter Set. He joined HP in 1967 upon getting his degree (Ingenieur Graduate) from the Ingenieurschule Esslingen, Germany. Outside of working hours, Walter spends much of his free time sailplaning in the Alps—he's both a licensed teacher and a licensed sailplane inspector. He and his wife have two children, 9 and 7.

SPECIFICATIONS
HP Model 8030A Cardiotocograph

Input Section

CARDIO socket accepts input connectors for fetal heart rate monitoring. Instrument automatically selects correct operating mode and performs signal calibration and sensitivity adjustments.

DIRECT FETAL ECG AND ABDOMINAL ECG
- INPUT SIGNAL RANGE: 10 μVp to 3 mVp.
- INPUT IMPEDANCE: ≥50MΩ (differential).
- NOISE: <2μVp (25 kΩ source resistance).
- COMMON-MODE REJECTION (with patient cable): ≥140 dB with 5 kΩ imbalance, 50-60 Hz.
- PATIENT ISOLATION: ≥40 MΩ dc to 60 Hz measured at 120 V.

ULTRASOUND
- ULTRASOUND INTENSITY: <10 mW/cm²
- FREQUENCY: 2.1 MHz.

HEART SOUND: Selective amplifier, high dynamic range (50 dB).

TOCO socket accepts connectors for intrauterine pressure and external labor monitoring. Instrument automatically selects correct operating mode and performs signal calibration and sensitivity adjustment. 10-turn front-panel control adjusts TOCO channel baseline; no other adjustment is necessary.

EXTERNAL LABOR
- SIGNAL RANGE: 0 to 1000 g.

INTRAUTERINE PRESSURE: (with Model 1286A Pressure Transducer)
- SIGNAL RANGE: 0 to 100 mmHg.
- NONLINEARITY: 1% of full scale.
- OVERLOAD PROTECTION: 3000 mmHg.
- PATIENT ISOLATION: ≥48 MΩ, dc to 60 Hz measured at 120 V.

Display Section

DIGITAL DISPLAY
- TYPE: 11-mm, 7-segment LEDs
- FETAL HEART RATE RANGE: Direct fetal ECG, 30-240 bpm; all other methods, 50-210 bpm.
- UTERINE ACTIVITY RANGE: 0-100 mmHg for intrauterine pressure, 0-100 relative units for external labor.
- ACCURACY (Ratemeter and Tocometer): ±0.5% of full scale ±1 digit.

INSTRUMENT DISPLAYS
- ACCEPTANCE LAMP: Flashes with each valid heart rate measurement.
- INOP LAMP: Lights when there is no patient cable or transducer connected to CARDIO input or, if in either ECG mode, an electrode makes poor contact. INOP also lights if cardiotocograph does not contain processing circuits for transducer that is connected.

STATUS INDICATORS: Appropriate indicator turns on to show monitoring method in use when transducers are connected to CARDIO and TOCO sockets.

Recorder Section

Two-channel, servo-driven recorder with contactless position feedback transducer.

CHART SPEEDS: 1 and 2 cm/min (optionally 1 and 3 cm/min).
CHART PAPER: Thermosensitive, Z-fold paper with numbered pages. Recording time: 24 hours at 1 cm/min.
STYLI: Thick-film heated styli; heat-up time: 20 ms.

FETAL HEART RATE (CARDIO) SCALE
- VERTICAL SCALE: 7 cm (with scale A) or 8 cm (with scale B).
- VERTICAL SCALE SENSITIVITY: 30 bpm/cm (scale A) or 20 bpm/cm (scale B).
- RANGE: 30-240 bpm (scale A) or 50-210 bpm (scale B).

UTERINE ACTIVITY (TOCO) SCALE
- VERTICAL SCALE SIZE: 4 cm.
- VERTICAL SCALE SENSITIVITY: 25 units/cm.
- RANGE: 0-100 units.

General

TEST BUTTON: Pressing TEST button produces 200 ±2 bpm in cardio channel and adds 50 in toco channel when there are no connections to instrument. Both values are displayed and recorded. When a transducer is connected, appropriate test signal also appears on CRT.

ECG TEST SOCKET (on front panel): in direct fetal ECG mode, enables complete front-end test of instrument, CRT, and patient cable.

REAR PANEL OUTPUTS: Analog outputs of fetal heart rate and uterine activity; amplified versions of original direct ECG, abdominal ECG, ultrasound, and heart-sound inputs; many other analog and digital signals for research purposes and testing. LOGIC switch disables artifact rejection logic (pen lift) to permit observation of arrhythmias.

OPERATING TEMPERATURE RANGE: 0 to 55°C.
POWER: 115 or 230 V, +10%, −15%, 50-60 Hz, 42 VA.
DIMENSIONS: 178 mm H × 425 mm W × 356 mm D (7 × 16.7 × 14 inches).
WEIGHT: 12 kg (27 lb).
PRICE IN U.S.A.: Model 8030A Cardiotocograph with direct ECG, ultrasound, and external labor transducers and processing circuits: $6250. With addition of abdominal ECG, add $850; heart sound, add $500, intrauterine pressure, add $650. Model 8031A Cardiotocograph: $5100; 8032A Repeater: $2650.
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