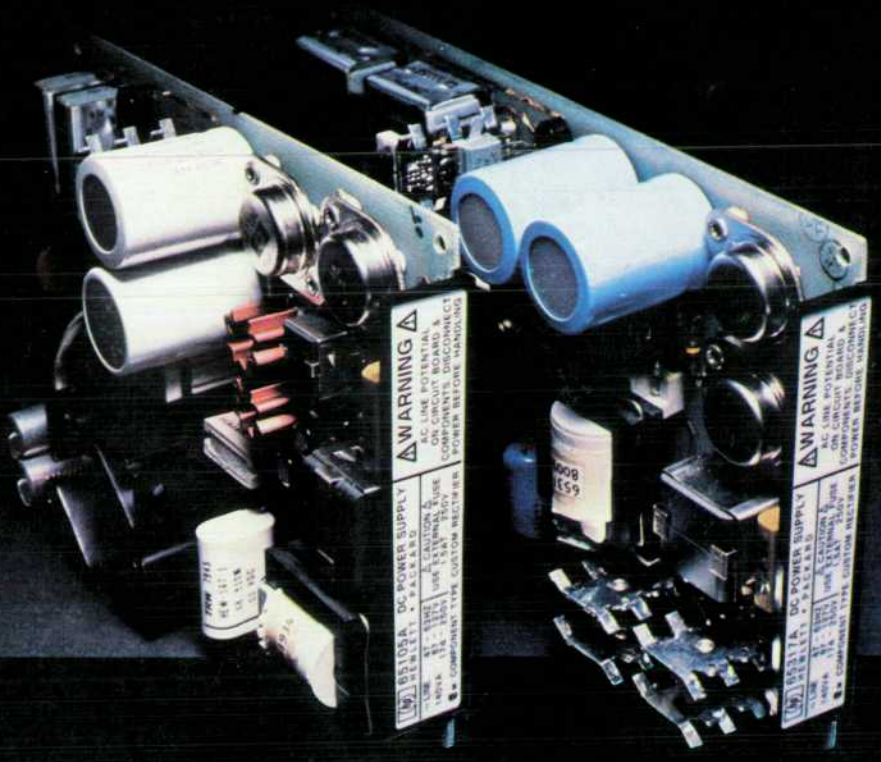
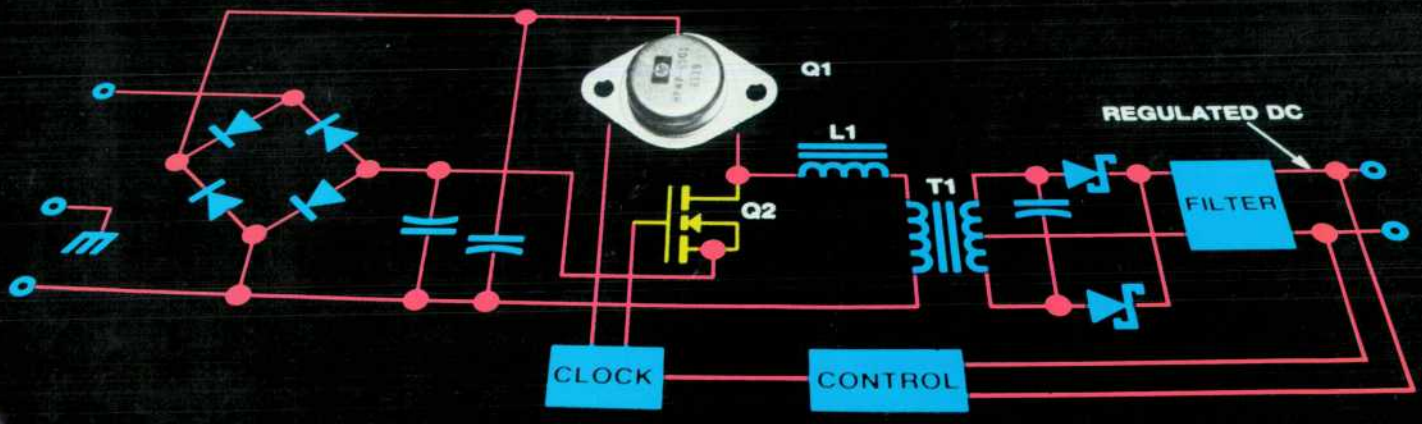
AUGUST 1981

HEWLETT-PACKARD JOURNAL





HEWLETT-PACKARD JOURNAL
Technical Information from the Laboratories of Hewlett-Packard Company

Contents:

AUGUST 1981 Volume 32 • Number 8

In this Issue:

When we plug something into an electrical outlet we are connecting it to a voltage that alternates between positive and negative values 50 or 60 times per second, depending on the country. This voltage may be subject to random noise and to large, unpredictable, sudden fluctuations as the utility company supplying us with electric power experiences demand variations, electrical storms, equipment problems, and other disturbances. Electronic circuits like those in television sets, computers, stereo systems, and electronic instruments don't like this kind of power. They need steady, well regulated, battery-like voltages. Large disturbances can disrupt or even destroy them.

The articles in this issue deal with the problems of changing unregulated alternating voltages to regulated battery-like ones, and of dealing with unpredictable power anomalies. The first two articles are about the design of some innovative new power supplies. Power supplies are electronic devices that convert what comes out of an electrical outlet to regulated voltages for other electronic devices to use. For example, there's a power supply inside every piece of electronic equipment. This kind of power supply should be small and as reliable as the wall outlet it's plugged into. The 65000A Series Modular Power Supplies (cover and page 3) are of this type. There are also power supplies that provide regulated voltages to circuits outside their own cabinets. These might be found sitting on a lab engineer's bench or mounted in a rack as part of a computer-controlled test system. These supplies should be extremely well regulated, accurate, and for some applications remotely programmable. Models 6012A and 6024A Autoranging Power Supplies (page 11) are in this category.

Although they are meant for different applications and represent different design approaches, both of these new power supply families take advantage of a new HP switching transistor called a power MOSFET (metal-oxide-semiconductor field-effect transistor). MOSFETs have been around for a while and their superiority over other kinds of transistors for many high-frequency applications is well known. However, until recently there weren't any with the HP device's combination of high voltage rating, fast switching speed, low resistance, high reliability, and small chip size. The cover photograph shows where the HP power MOSFET fits in the schematic diagram of a 65000A Power Supply. On page 18 is an article about the new MOSFET, telling why it's different and how it's made.

The special problems power line disturbances cause computers (in spite of their well regulated power supplies) are discussed in the article on page 25. This article is based on studies of typical power line conditions, wiring codes for buildings, computer installation procedures, and computer designs. The article should be of interest to anyone who owns a computer system or is considering installing one.

-R. P. Dolan

200-kHz Power FET Technology in New Modular Power Supplies

These small, reliable 50-watt supplies are designed for OEM (original equipment manufacturer) use anywhere in the world.

by Richard Myers and Robert D. Peck

A NEW HP-DEVELOPED fast-switching power field-effect transistor (FET) has made possible a new series of 50-watt printed-circuit-board power supplies that feature very small size, light weight, and demonstrated reliability of 100,000 hours mean time between failures (MTBF). Fig. 1 shows some of the eight models in the 65000A Series. They have one to six outputs in combinations of 5, 12, 15, and 18 volts dc. Intended for worldwide use, the supplies operate from both 120Vac and 240Vac power lines. They are UL-recognized in the U.S.A. (UL 478 and UL 114), certified by CSA in Canada (CSA 22.2 No. 143 and No. 154), and are designed to meet the requirements of VDE in the Federal Republic of Germany (VDE 0730 Part 2P) and IEC 348. They are brownout-proof and have remote shutdown terminals.

These power supplies are designed for use by original equipment manufacturers (OEMs) in modems, flexible disc drives, microcomputers, and many instruments. They meet OEMs' usually contradictory requirements for power supplies. For example, OEMs want low levels of electromagnetic interference (EMI) and conformance to safety regulations along with small size and weight. However, with most circuit schemes, meeting domestic and international EMI and safety requirements means large size and weight to accommodate EMI suppression components and safety spacings between and within components. OEMs also want complex system features such as remote shutdown and overvoltage, overcurrent, and overtemperature protection along with reliability and well regulated dc output voltages. Providing these features conventionally means complex circuits and therefore inherently lower reliability.

Design Approach

The key ingredients that make it possible to meet these usually conflicting requirements are power MOSFET* technology, a switching frequency of 165-200 kHz, and sine-wave power conversion.

HP has been designing and manufacturing conventional switching-mode power supplies for many years and their peculiar problems are well understood. For all their virtues, they suffer from several notable difficulties. They are capable of producing high levels of EMI, have complex timing requirements, particularly during turn-on and turn-off transients, and as a result are susceptible to catastrophic faults, and have resisted attempts to increase their frequency of operation beyond 50 kHz. Higher operating frequencies have been a temptation for several years; however, switching transistors suitable for operating frequencies beyond 50 kHz and operating voltages of 450V have not been readily available. Yet small size requires a much higher switching frequency.

Power MOSFETs were the needed solution. A program

*Metal-oxide-semiconductor field-effect transistor.

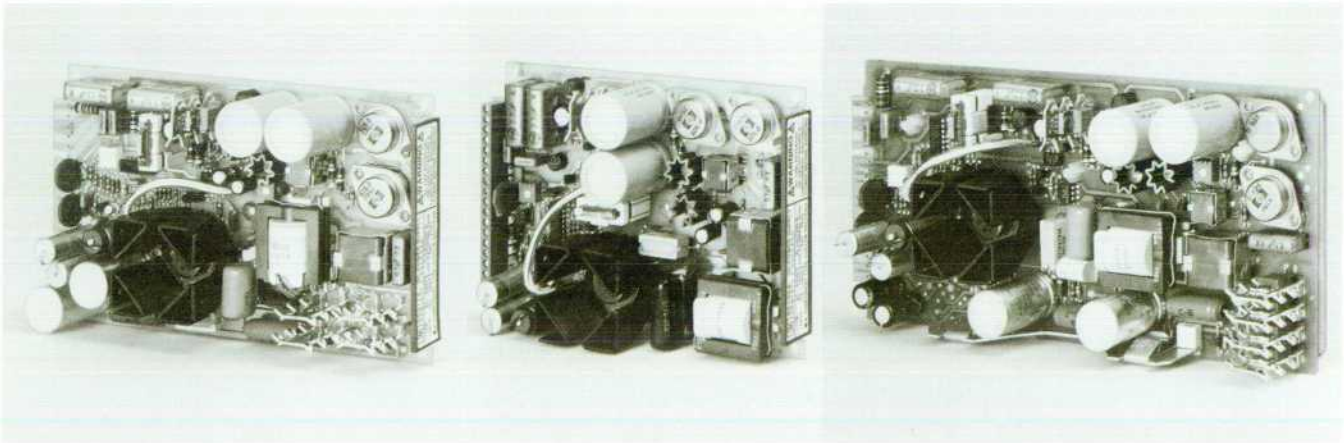


Fig. 1. *HP 65000A Series Modular Power Supplies are small 50W dc supplies that have one to six outputs in combinations of 5, 12, 15, and 18 volts. The eight models in the series meet worldwide safety and EMI standards and are highly reliable.*

was begun at HP to develop power FETs with characteristics suitable for off-line switching regulators (see article, page 18). However, it then became apparent that power switches were only part of the high-frequency problems. The construction of transformers that simultaneously meet worldwide safety requirements and have leakage inductance commensurate with standard pulse-width modulation techniques is no small matter. High-frequency operation of transformers in a conventional pulse-width modulation mode is difficult to achieve. If a transformer is designed to be thermally limited (fixed temperature rise) and its frequency of operation is increased, the per-unit leakage inductance of the transformer increases approximately as the square root of the frequency. Leakage inductance results in power dissipation in snubber circuits, EMI, increased open-loop output impedance, and increased stress on power semiconductors. Clearly, if high-frequency operation is desired some method of eliminating the undesirable effects of leakage inductance had to be found.

Sine-Wave Voltage Regulation

The power conversion and voltage regulation technique used in the 65000A Series eliminates many of the bad effects of leakage inductance. 165-to-200-kHz square waves are converted to sine waves as an integral part of the regulation process. This voltage regulation technique can be explained with the circuit shown in Fig. 2. The circuit is a simple series resonant tank, and the voltage source E_g is a square-wave generator. The low-pass characteristic of the tank circuit effectively filters the square wave and converts it to a sine wave.

For the purpose of analysis consider the source to be a sinusoidal source whose output is equal to the magnitude of the fundamental component of the square wave. This approximation allows routine ac analysis to be used and simplifies the mathematics considerably. R_L represents the load connected to the output of the power supply, plus rectifier, switch, and magnetic losses. L and C are the energy storage elements of the resonant tank.

If the frequency of the generator, f_g, is equal to the resonant frequency of the tank and resistor R_L is sufficiently large, then the output voltage across R_L is a maximum. As the frequency of the generator is increased the output voltage falls asymptotically at 12 dB/octave, as shown in Fig. 3. If the generator is a voltage-controlled oscillator (VCO) whose minimum frequency of operation is the resonant frequency of the tank, the output voltage developed across R_L is easily controlled. Rectification and filtering of this output voltage generates the required dc output. As the load current drawn from the power supply decreases, the Q of

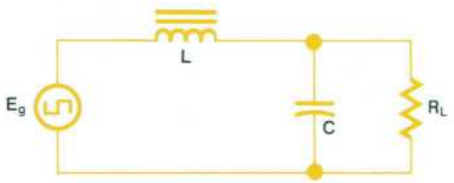


Fig. 2 *This simplified circuit illustrates the voltage regulation technique used in the 65000A Series Power Supplies. The tank circuit converts the square wave to sine waves as an integral part of the technique. See Fig. 3.*

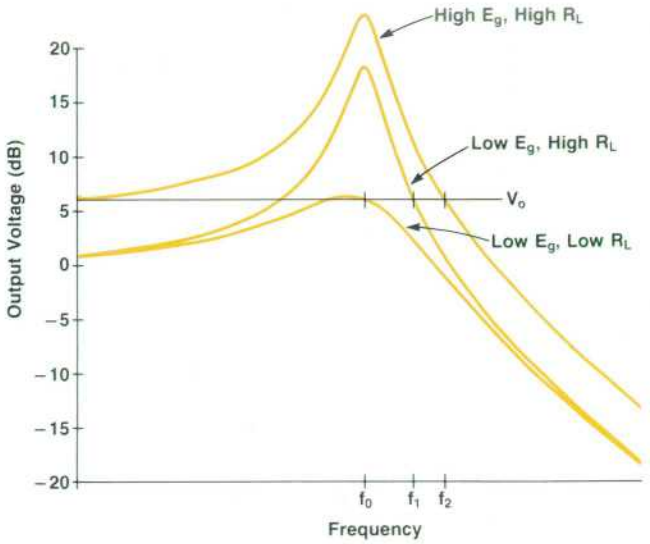


Fig. 3. *Transfer function for the circuit of Fig. 2. Adjusting the frequency of the generator keeps the output voltage constant at V_o under varying line voltage and load conditions.*

the resonant tank increases and the control circuit increases f_g, thus maintaining a constant output voltage.

Significantly, if the output is short-circuited (R_L=0) the output current and the current in E_g are limited by the resonating inductor L. This inherent current-limiting mechanism is of great value in controlling faults and in simplifying control circuits.

Compared to the usual pulse-width-modulation switching regulated power supply, this sine-wave power conversion technique requires 25-33% fewer control and drive components. It also provides 15-20 dB less EMI than typical 50-to-100-watt open-frame switching power supplies.

Power Supply Circuit

An implementation of this circuit for voltage regulation is shown in Fig. 4. It is shown operating directly from a 120Vac 60-Hz power line. After conversion from 60-Hz ac to unregulated dc, the dc output voltage is regulated by the method shown in Fig. 3.

In this circuit a bridge-doubler capacitor configuration is used to derive a ±160Vdc supply from the ac power line. This voltage is unregulated and contains a significant percentage of 60-Hz and 120-Hz ripple. Power FETs Q1 and Q2 provide the square wave by switching alternately.

The use of FETs is not arbitrary. Conventional bipolar transistors present very difficult problems because their storage time makes simultaneous conduction of Q1 and Q2 a certainty if they are driven with square waves (see Fig.4). Pulse-width modulators used in conventional switching supplies avoid square waves by inserting a dead time. Unfortunately, this use of dead time increases the complexity of the driver circuit. Because FETs do not have storage time, they can use a square wave and a simple drive circuit, with a reduced parts count and a consequent increase in reliability.

In Fig. 4, L1 is the resonating inductor and serves to insure that the voltage applied to transformer T1 is truly sinusoidal. Since the voltage rate of change (dv/dt) applied

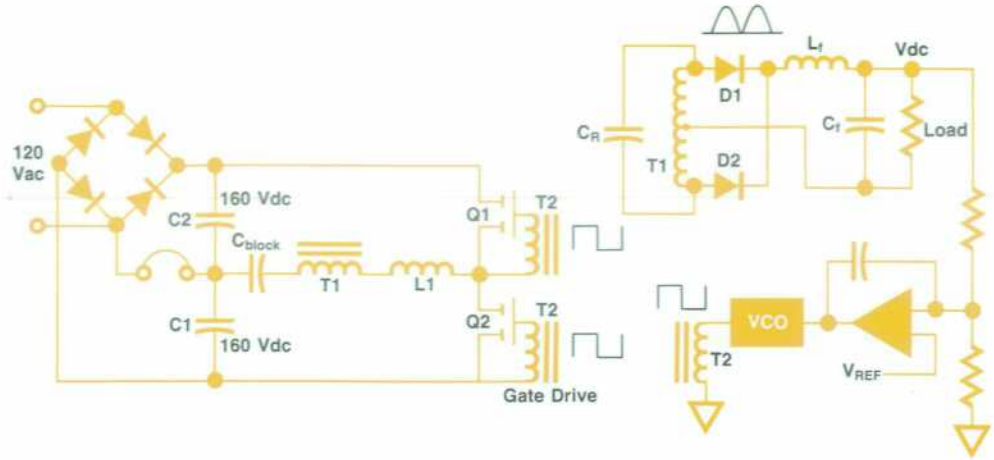


Fig. 4. *Simplified schematic of a 65000A-type off-line sine-wave converter.*

to the transformer is significantly reduced by L1, the problem of EMI is dramatically lessened. C_{block} serves to insure that no dc current is allowed to circulate in T1. C_R, the resonating capacitor, appears on the secondary of transformer T1. Notice that this placement of C_R effectively puts the leakage inductance of transformer T1 in series with resonating inductor L1. A price is paid, however, for this tuning out of the leakage inductance. The rms current in the resonating capacitor is nearly the same as the dc output current. This made it necessary to develop high-current capacitors for the 65000A Series, as discussed later in this article.

Rectifiers D1 and D2 and the output filter (L_f and C_f) constitute a conventional center-tapped full-wave rectifier and averaging filter. Significantly, the required inductor L_f is smaller than an equivalent filter inductor in a pulse-width modulator by a factor of nearly 2.5 to 1. This reduction is possible because sine waves are being filtered instead of a pulse train.

The filtered output voltage V_{dc} is compared to the desired output voltage V_{REF}, amplified and applied to a voltage-controlled oscillator. The oscillator is used to drive the power FETs and regulate the output voltage. A special magnetic component developed for the oscillator allows the frequency of a square-wave oscillator to be controlled by varying the current in a winding. This control inductor was selected because of its simplicity, reliability, and ability to meet worldwide safety standards.

Several characteristics of this power supply circuit make it especially attractive for use in the 65000A Series. It uses a simple and reliable control technique with standard linear circuits and without recourse to complex and unwieldly pulse-width circuits. It has inherent current limiting that requires no additional circuitry. A short on the output rectifiers, resonating capacitors, or transformer will actually produce a decrease in the FET current.

High-frequency operation can be easily achieved. The 65000A Series operates at frequencies in excess of 200 kHz and is designed to meet worldwide safety specifications. The output choke in the output averaging filter is 2.5 times smaller than an equivalent choke in a pulse-width modulated unit. EMI problems are minimized because of the presence of sinusoidal waveforms at all points beyond the resonating inductor L1. The simple control techniques result in a lower parts count and a much improved MTBF (greater than 100,000 hours MTBF demonstrated for a single-output unit with 395,000 unit hours of life tests).

The disadvantage of the circuit is that it requires an extra magnetic component (resonating inductor L1) and a resonating capacitor C_R. However, this disadvantage is more than compensated by the sharp reduction in size resulting from the increased frequency of operation (almost 10:1).

Voltage-Controlled Oscillator

The novel voltage-controlled oscillator provides more than one ampere of drive current to the FETs using only eight components. It is an inductively coupled, astable multivibrator. A simplified circuit diagram is shown in Fig. 5.

To understand the oscillator's operation assume that transistor Q4 is conducting. The current I_{TS} is equal to $(KV_{CC} - V_{BE})/R_S$ and is constant. Because V_{BE} is positive, transistor Q5 is held off and voltage V_{CC} is applied to the primary of transformer T1. The voltage $V_L(t)$ is positive and results in an increasing current $i_L(t)$ and eventually $I_{TS} =$

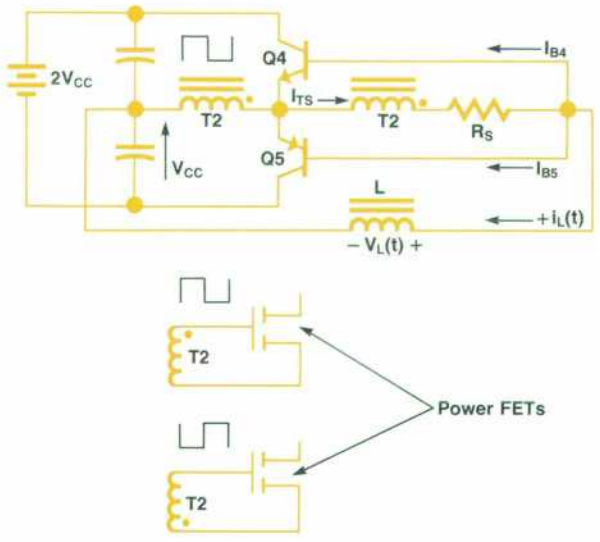


Fig. 5. *High-current voltage-controlled oscillator (VCO) provides more than one ampere to drive the power MOSFETs, using only eight components. L is a variable control inductor; the oscillator frequency is controlled by varying the inductance of L.*

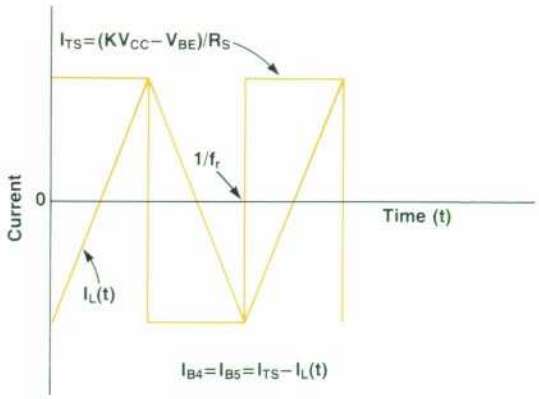


Fig. 6. *Current-time relationships in the voltage-controlled oscillator of Fig. 5.*

$i_L(t)$. This results in zero base current for Q4, which forces it to turn off regeneratively. Since $i_L(t)$ is still positive, transistor Q5 is turned on very hard, resulting in a sharp voltage transition on transformer T2. Fig. 6 shows the current relationship.

The frequency of operation of this oscillator is given by the expression

$$f_r \approx \frac{R_S\ (V_{CC} + V_{BE})}{4L\ (KV_{CC} - V_{BE})}$$

Notice that because Q4 is turned off completely before Q5 is turned on, there is no possibility of simultaneous conduction of transistors Q4 and Q5. As a result, this oscillator is capable of driving heavily capacitive loads with a very respectable square wave at frequencies in excess of 200 kHz. The frequency of the oscillator is varied by controlling the effective inductance L. This variable control inductor appears schematically in Fig. 7. An especially useful feature of the variable control inductor is that very little of the ac voltage generated on the primary of the inductor (the oscillator side) is reflected to the control winding. The variable control inductor is described in more detail on page 8.

Power FET gates make good loads for drive circuits because of their high impedances. In addition, FETs eliminate concern about storage time. As a result, a FET drive circuit is very simple, as shown in Fig. 8. The resistor-diode networks in the drive circuit provide a small delay between turn-on and turn-off of the power FETs. This helps reduce switching losses.

Simplified Power Supply Schematics

The simplified schematic of Fig. 9 shows a single-output supply. The 320V peak-to-peak square wave output from Q1 and Q2 drives the series resonant circuit consisting of inductor L1, the leakage inductance of transformer T1 and the reflected capacitance of capacitor C_R. The nominal frequency of the clock driving the FETs is higher than the circuit's resonant frequency. Regulation is by frequency modulation. When the control circuit slows down the clock and the FET switching rate, the voltage across capacitor C_R increases and thus increases the rectified and filtered output voltage V1. When the clock speeds up, output voltage V1 decreases. The control circuit adjusts the frequency to provide 0.1% line and load regulation for V1.

The schematic of Fig. 10 shows how multiple output voltages are implemented and how 120/240Vac dual power line capability is included. Fig. 10 also shows the bias supply and protection circuitry.

Output voltages V2 through V5 of this multiple-output model are derived as shown in the lower right of the figure. Semiregulated outputs V2 and V3 are the rectified and filtered outputs from an extra secondary winding on transformer T1. Outputs V4 and V5 are powered by V2 and V3 and provide 2% line and load regulation. The resonating capacitor function is now shared by two capacitors, C4 and C5.

Fig. 7. *Simplified schematic of the variable control inductor shown in Fig. 5.*

Power FETs

The power FET and the 65000A Series Power Supplies were developed together. When the 65000A project began only one power FET was being developed commercially and it was low-voltage (90V), extremely expensive, and had both reliability and delivery (manufacturing) problems. The requirements for a high-voltage (450V) power FET were analyzed by HP's central research labs, and it was concluded that the necessary production technologies existed and that FETs could be competitive with high-voltage bipolar transistors. The design and manufacture of a series of power FETs began at the central research labs.

The New Jersey Division assisted by setting up HP's first TO-3 packaging operation, by designing and building the high-voltage test equipment, and by setting up reliability test equipment for power semiconductors. Recently the Microwave Semiconductor Division has picked up responsibility for design, manufacture and packaging of the power FETs and now has its own test and reliability evaluation equipment.

The design and development program for the power FET

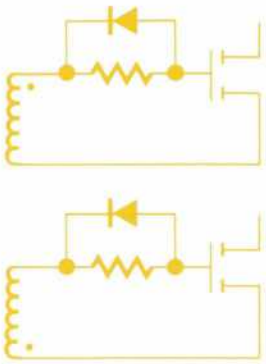


Fig. 8. *Power FET drive circuit can be very simple because the FETs have high impedance and no storage time problems.*

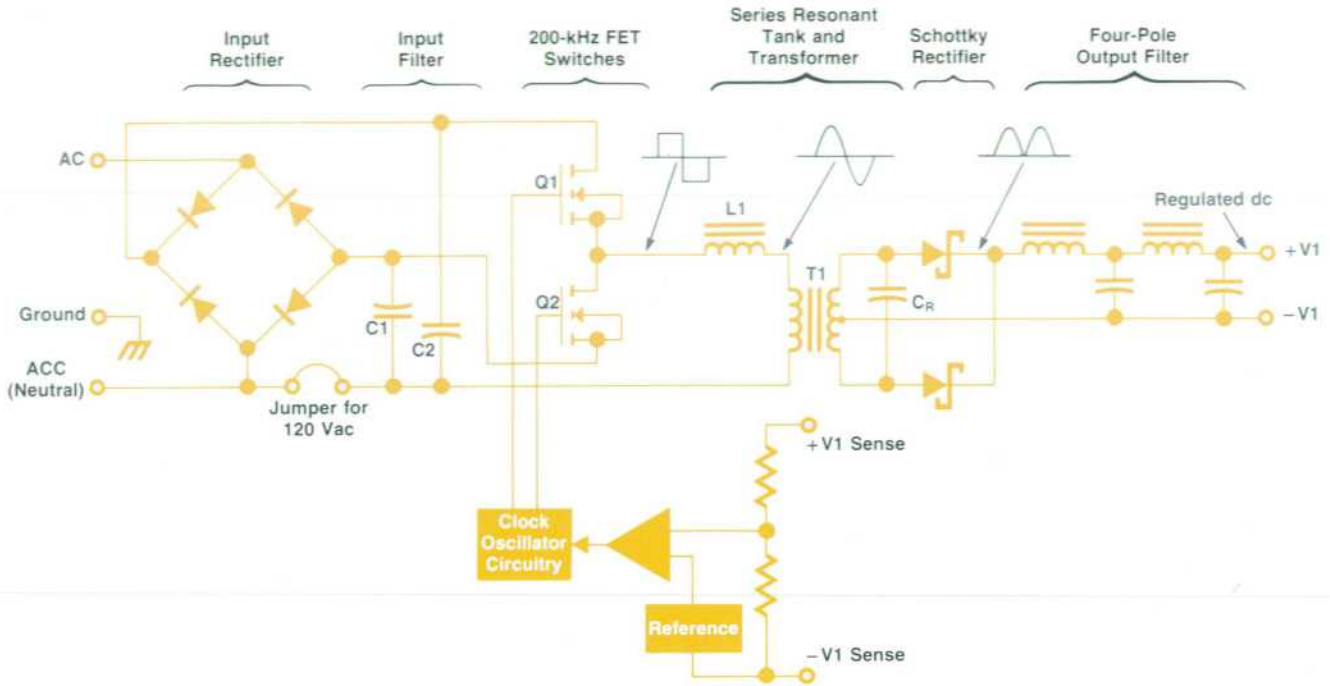


Fig. 9. *Simplified schematic of a single-output 65000A Series Power Supply.*

was different from a development program for a typical high-voltage power transistor. The performance of a FET can be accurately predicted and so the extensive experimentation and redesign that characterize bipolar development programs were not necessary. Along with predictable performance, manufactured FETs have consistent gains and switching speeds. Consistency and predictability are major advantages of FETs over bipolar power transistors and were crucial in the decision to develop a power FET just for switching power supplies.

While the electrical performance was predictable, the challenge for the research labs was to develop HP's first high-voltage manufacturing process and make reliable FETs. A high voltage rating of 450 volts is necessary for any off-line power supply designed to operate from 240Vac as used in Europe. A high voltage rating requires high-resistivity silicon, which leads to high on resistance. Since high on resistance is undesirable, the FET production process has to be precisely controlled so that every FET has a voltage capability that is high enough, but not too high—470 to 530 volts is the permitted range. Another problem is that high voltages cause strong fields inside the FETs. These fields move any mobile ions present and thus change the threshold voltage and increase the drain leakage current, possibly causing power supply failures. Mobile ions can result from contamination, so the FET manufacturing process must be very clean to reduce their number.

From the beginning of the project reliability was a major concern. A reliability demonstration of 500,000 hours was required before the FETs would be used in the 65000A Series Power Supplies. The time required for the demonstration was compressed by a factor of about 25 by testing at 175°C instead of the 125°C maximum temperature rating. After considerable effort by the research labs, the FETs passed the 1000-hour test with just two failures in 140 devices. With each process change by any vendor these tests are repeated. Samples are taken from lots and given similar reliability tests. In this way continuing reliability is assured.

The power FETs have met the original goals. They have the required voltage, low on resistance, fast and consistent switching speeds, consistent gains, good manufacturing yields, and reliability. This contrasts with and is a welcome improvement over the performance of high-voltage bipolar transistors.

Film Capacitors

The resonant circuit regulation scheme of the 65000A Series calls for a high-current film capacitor. The current in the capacitor is about 90% of the output current. This capacitor, required on the secondary of transformer T1 (C_R in Fig. 4), is physically large. Its operating current approaches the wire lead current rating and exceeds most manufacturers' current ratings for the capacitor winding end connections.

There were no commercially available capacitors with sufficient current ratings. Because the capacitor in the resonant circuit has sinusoidal voltage and current waveforms, it was reasonable to expect that conventional low-cost film capacitors would be reliable. HP provided capacitor manufacturers with test circuits to demonstrate successful sine-wave operation at high currents. Life tests were begun at HP to explore the possibility that new and unexpected failure mechanisms could be introduced by the high currents. These tests demonstrated that temperature was the prime concern and reliability required just careful thermal design. The capacitor type finally approved uses film-foil construction and polypropylene dielectric. Low-loss polypropylene capacitors and solid copper leads soldered directly to the foil in the capacitors met the reliability re-

(continued on page 10)

Magnetic Components for High-Frequency Switching Power Supplies

by Winfried Seipel

Designing magnetic components for operation at 200 kHz requires careful consideration of the properties of materials beyond any normally required at much lower frequencies. Each of the major magnetic components in the 65000A Series presented a different set of problems requiring resolution. Our goals were to develop components small in size, design to meet the most stringent of European safety specifications, and allow for the possibility of semiautomated manufacturing to reduce manufacturing costs. The magnetic components of major interest are the resonating inductor, the control reactor (variable control inductor), and the power transformer.

Resonating Inductor

The resonating inductor, Fig. 1, is an ac device that carries the primary circuit resonating current. It was designed using a printed-circuit-mountable coil form and the core was chosen to provide some measure of self shielding. Losses in the device are minimized by operating the core at a flux level appropriate for the ferrite material selected and by selecting a suitable litz wire* for the winding. To determine the proper flux level the actual core losses for the core selected had to be determined. Published data is generally valid only for specific shapes. It is important to note that core losses are dependent not only on material properties but also on core geometry. The second concern was the selection of the magnet wire. Litz wire is an obvious choice. However, too many strands of very fine wire are expensive and counterproductive, because the percentage of the total volume that is insulation climbs very rapidly as the magnet wire gets finer. If a given volume is available for wire, that volume can very quickly become virtually solid insulation. However, two few strands of a heavy wire will experience an unacceptable increase in resistance because of proximity effect. Although proximity effect is a function of skin effect, or more precisely skin depth, the effect can be orders of magnitude worse. Proximity effect is a function of skin depth, conductor diameter, turns per layer, number of conductors per turn, and the number of layers in the coil. The increase of coil resistance from this effect occurs because the magnetic field surrounding each wire in the coil cuts through every other wire in the coil, thereby generating eddy currents. These eddy currents add to and subtract from the normal circuit current to produce a very distorted current distribution.

One additional difficulty required consideration. The air gap in the core structure necessary to adjust inductance properly and prevent saturation causes a large fringing flux through the coil section adjacent to the gap. The fringing flux causes additional coil losses through the generation of additional eddy currents in the wire.

*Litz wire is a type of twisted stranded conductor in which the individual strands are insulated separately.

Control Reactor

The control reactor specifications were such that a totally different set of problems from that encountered with the resonating inductor had to be resolved. The device, shown in Fig. 2, is essentially a saturable reactor but with a considerably more gradual saturating characteristic than is normally associated with such a device. It consists of two series-connected reactor coils and one control coil on a pair of E-shaped cores. The control coil is on the center leg and a reactor coil is on each of the outer legs. By the application of a current to the control coil, the impedance of the series-connected reactor coils can be varied. The initial inductance of the reactor is specified to be not less than a certain value given the realities of production and material tolerances. With the application of a specific current to the control winding, the inductance of the reactor coils had to be of a value not greater than a specified amount. In addition, the signal normally fed back to the control coil from the reactor coils in a series-connected device had to be negligible. The design of the device involved the selec-

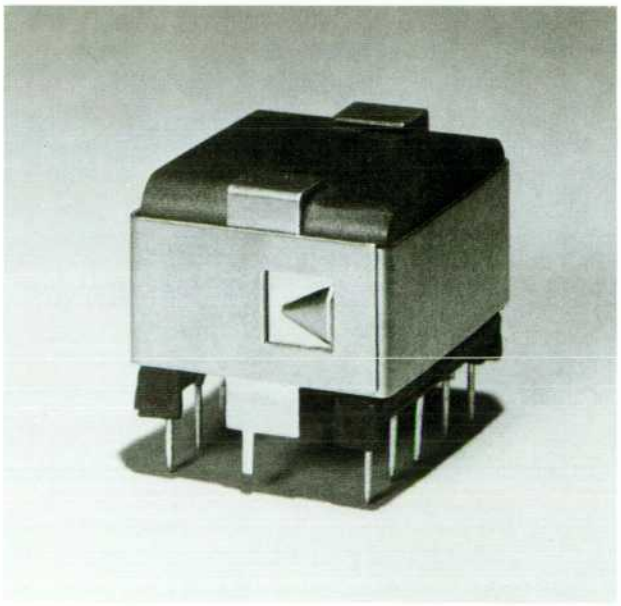


Fig. 1. *Resonating inductor.*

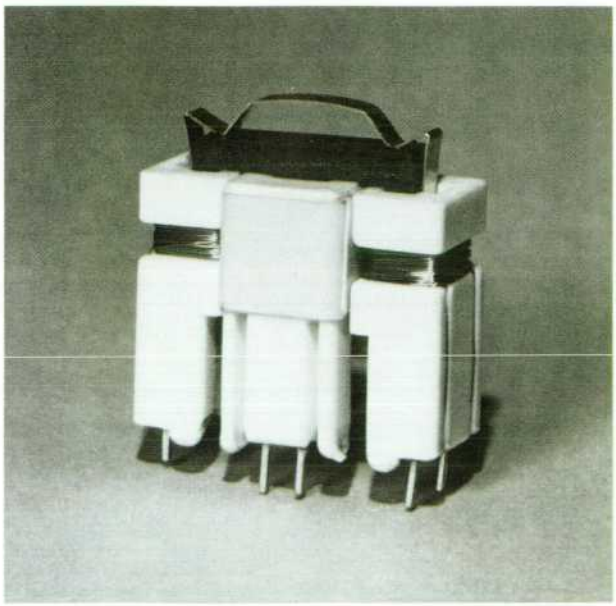


Fig. 2. *Control reactor (variable control inductor).*

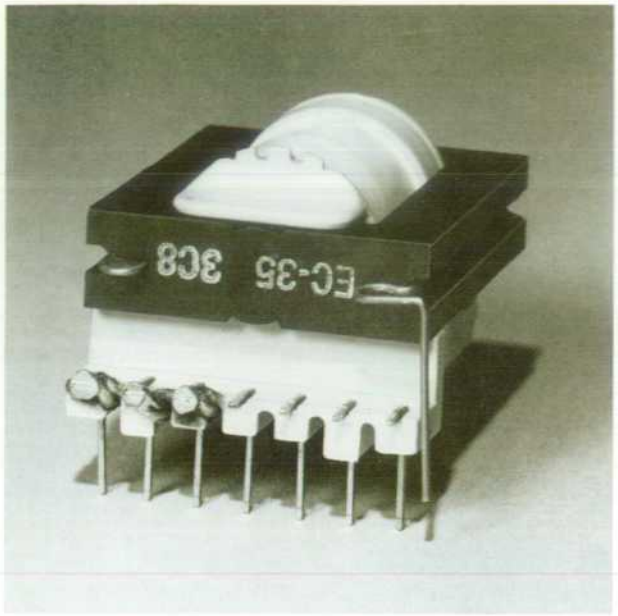


Fig. 3. *Power transformer.*

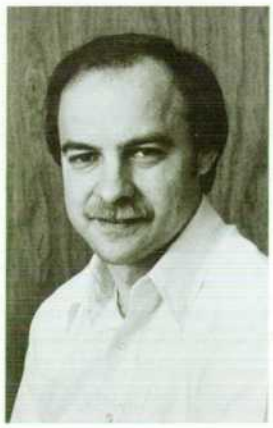
tion of an E core manufactured with a very high-permeability material in a size such that turns and operating flux density could be minimized. Using a high-permeability core material, thereby minimizing reactor turns to achieve the required initial inductance, resulted in minimizing control current requirements. Minimizing control current is extremely important since the availability of this current is severely limited. By keeping the operating flux density in the outer legs of the control reactor low, the legs are essentially kept always in balance. Any flux change in one reactor leg also occurs in the other, thereby preventing flux from being diverted to the control leg. In a typical high-flux reactor, one leg is in saturation while the other is in the linear region. This results in an ampere-turn balance between one and then the other unsaturated reactor coil and the control coil, resulting in an unwanted ac current in the control loop.

An interesting and unusual problem surfaced in the development of this device. Because it is in the feedback path of the control circuit of the power supply, any changes of inductance not related to changes of control signal represent a disturbance for which the control circuit has to compensate. In other words, any mechanical changes in the reactor result in inductance changes, which can result in an unstable circuit. Not only do the core halves have to be securely held together, but any movement of the coils is also unacceptable.

Power Transformer

The problems encountered during the design of the power transformer, Fig. 3, were similar to those experienced in the development of the resonating inductor. Although the power transformer does not have an air gap in its core structure, it does have to carry significantly higher currents in its secondary windings. Due to the creepage and clearance distance and insulation thickness built into the unit, the leakage inductance is fairly high. The use of litz wire with the correct stranding and wire gauge for winding the primary coil is a fairly straightforward solution to minimizing primary coil losses. Litz wire is also used where the secondaries are of the higher-voltage type. However, for the low-voltage winding at the five-volt level, litz wire is impractical, and copper strip is the solution. For the few turns required to provide the necessary secondary voltage, copper strip is the best choice. In the presence of high leakage inductance, more copper losses than would normally be expected occur, because of eddy currents generated by the leakage flux passing through the surface of the strip. Copper strip also suffers from proximity effect but to a lesser degree than litz wire. The same factors as outlined for the resonating inductor govern the magnitude of the effect for strip. Considering the additional losses caused by leakage fields the right combination of strip width and thickness had to be determined.

As in the case of the resonating inductor, core losses had to be determined for the geometry used so that the proper flux level could be found. At 200 kHz the percentage of the total core losses attributable to eddy currents is significant, and eddy currents are a function of geometry.



Winfried Seipel

Win Seipel joined HP's New Jersey Division in 1969 after receiving his BSEE degree from Newark College of Engineering. His responsibilities have included the design and development of magnetic components, and more recently the management of the magnetic component design group. His work has resulted in a patent on a self-commutated SCR power supply. Born in Nordenham, Germany, Win enjoys chess and radio controlled model airplanes. He's married, has a daughter, and lives in Lebanon Township, New Jersey.

Richard Myers

Rich Myers graduated from Drexel University in 1962 with a BSEE degree, and began his career as an applications engineer for power transistors and related products. He joined HP in 1973 as a development engineer and helped design 500W, 300W, and 50W switching power supplies, including the 65000A Series. He's now a materials engineer with HP's New Jersey Division and is a member of IEEE. Rich was born in Williamsport, Pennsylvania and now lives in Somerville, New Jersey. He has two children and enjoys reading, travel, and home projects.

Robert D. Peck

Bob Peck received his BSEE degree in 1965 from New Jersey Institute of Technology. After two years in the U.S. Army and two years in electronic design, he joined HP's New Jersey Division, contributed to the design of the 62605J and 63000 Power Supplies, and initiated the design of the 65000A Power Supplies. His work has resulted in a patent on a limit cycle controller. Born in Queens, New York, Bob is married, has two children, and lives in Oakridge, New Jersey. He enjoys chess, bicycling, and hiking.

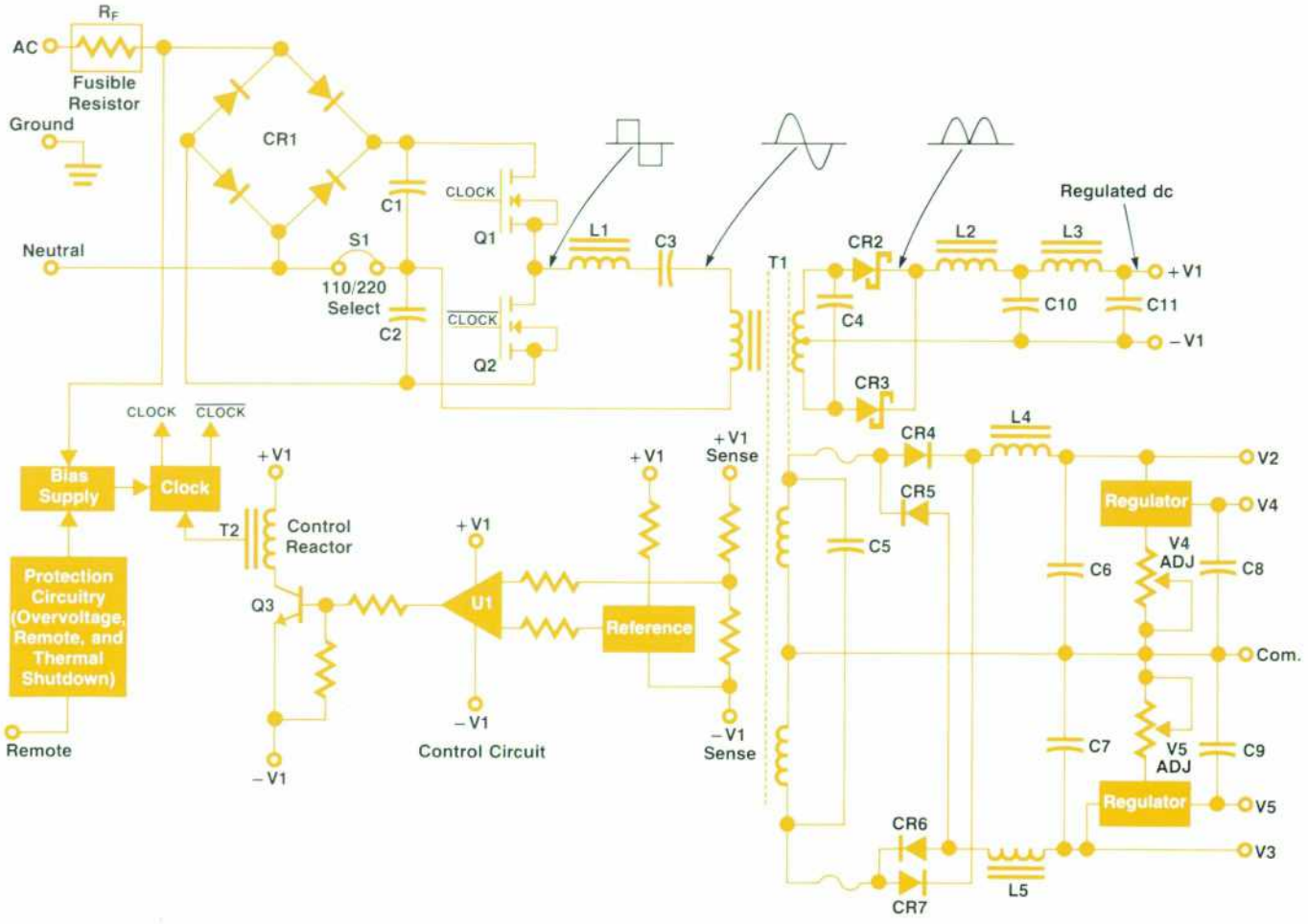


Fig. 10. *Simplified schematic of a five-output 65000A Series Power Supply.*

quirements for these power supplies.

Rectifiers

The choice of 200 kHz for the operating frequency was no problem for Schottky rectifiers, but the 65000A Series was expected to provide outputs of 15 volts and more, where Schottky rectifiers could not be used or economically justified. The sinusoidal voltage waveform makes the reverse recovery characteristics less critical. Since a reverse recovery time t_{rr} of less than 200 ns is considered necessary for 20-kHz power supplies, one might expect that at 200 kHz, rectifiers with a reverse recovery time less than 20 ns would be needed. Instead, at 200 kHz with sine-wave voltages the new low-cost 50-ns rectifiers are quite adequate. In other words, the required t_{rr} is reduced by only a factor of four even though the operating frequency is ten times higher. Thus low-cost 50-ns rectifiers can be used instead of high-cost 20-ns devices. These 50-ns rectifiers are available at voltages up to 150V, sufficient for 48Vdc outputs.

Acknowledgments

A large number of people contributed to the design and early production of the 65000A. John Kenny contributed to the electrical design. Mechanical design was by George Kononenko. Techician Pete Graziano put in many extra hours. Special credit is due Tim Kriegel as project leader for pressing the project through to completion, Dilip Amin for his circuit design contributions, and Win Seipel for the design of the magnetic components.

Laboratory-Performance Autoranging Power Supplies Using Power MOSFET Technology

State-of-the art components and circuit design enable this new generation of laboratory and system supplies to set new standards for performance and flexibility.

by Dennis W. Gyma, Paul W. Bailey, John W. Hyde, and Daniel R. Schwartz

TWO NEW AUTORANGING dc power supplies are the first of a new family of precision power supplies based on power MOSFET technology and designed for a variety of laboratory, industrial, and systems applications. Model 6024A (Fig. 1), rated at 200 watts, and Model 6012A (Fig. 2), rated at 1000 watts, deliver rated power over a 20-to-60-volt range, which is why they are termed autoranging. The 6024A will supply a maximum voltage of 60 volts and a maximum current of 10 amperes, but is limited to 200 watts. The 6012A will supply a maximum voltage of 60 volts and a maximum current of 50 amperes, but is limited to 1000 watts. The power supplies' output characteristics are shown in Fig. 3.

These power supplies have a wide variety of applications owing to the flexibility of the autoranging characteristic. On the laboratory bench or in an automatic system, a single supply can satisfy many different biasing requirements. This makes these supplies economically attractive for applications with changing or conflicting requirements, since they are comparable in price to supplies that give maximum power at only one operating point.

The 6024A and 6012A are notable in that they are switch-

Fig. 1. *Model 6024A is a 200-watt autoranging dc power supply. It uses high-frequency switching technology to provide expanded capability in systems and laboratory applications.*

Fig. 2. *Model 6012A is a 1000-watt autoranging dc power supply similar in design to the 6024A shown in Fig. 1.*

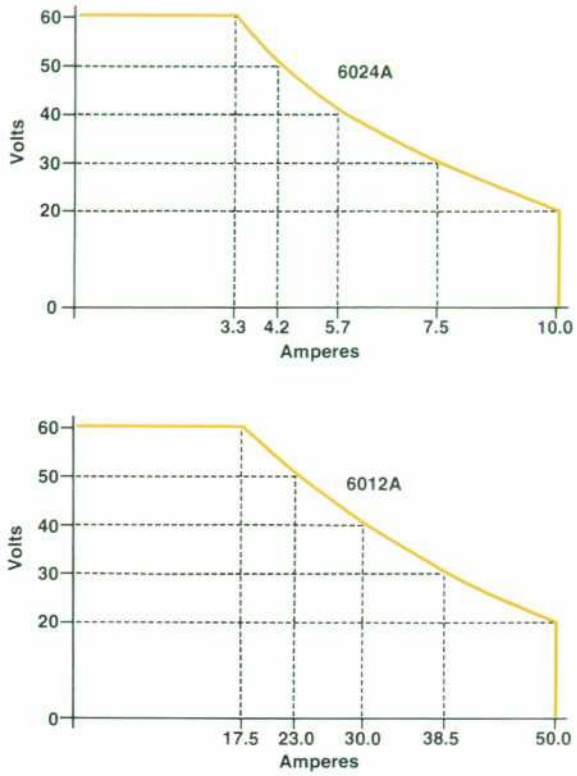


Fig. 3. *Output characteristics of the 6012A and 6024A power supplies. The curves show maximum output voltage as a function of output current and vice versa.*

ing regulated power supplies that achieve laboratory performance. They feature typical energy efficiencies of 80%, a 3-to-1 weight reduction over comparable series regulated units and an order of magnitude increase in programming speed at light loads. Output noise and line and load regulation are at the millivolt level. In addition, both products meet VDE regulations for conducted and radiated electromagnetic interference.

Both products provide such features as overvoltage and overtemperature protection, ten-turn front-panel adjustments for high resolution, and two analog meters for front-panel voltage and current display. Provision is made at the rear barrier strip for remote voltage or resistance programming in both constant voltage (CV) and constant current (CC) operation. Programming requires 0 to 5 volts or 0 to 2500 ohms for zero to full-scale output in either mode (CV or CC). Also present at the rear barrier strip is a current monitor output that provides 0 to 5 volts for zero to full-scale output current.

Switching Technology

The basic topology used in the 6024A and 6012A is the flyback converter (see block diagram, Fig. 4). This topology allows ready control of how much energy is stored in the magnetic field of the power transformer during each clock cycle. The converter operates at constant frequency and regulation is achieved by pulse-width modulation. An operating frequency of 20 kHz allows a dramatic reduction in component size and weight from 60-Hz series-regulated technology, making the products lighter and easier to manufacture. The operating frequency is above the audible range but not high enough to cause power dissipation problems with fixed losses throughout the converter section.

The ac line is brought in through both common-mode and normal-mode EMI filtering. Bias voltages are developed with standard 60-Hz techniques, and power is provided to the inverter through the inrush current limiting section. (Inrush limiting is achieved with thermistors in the 6024A and with limiting resistors shunted by a relay in the 6012A). Following the inrush limiting circuitry is a rectifier/filter section, which is configured as a voltage doubler for 100/120Vac operation and as a bridge for 220/240Vac operation. An unregulated dc bus voltage of approximately 300 volts is developed at the output of the rectifier/filter section.

Power FETs Q1 and Q2 are in series and are operated in-phase. The FETs are turned on by the pulse-width modulator, initiating linear current buildup in the magnetizing inductance of power transformer T1. Thus energy is stored in the magnetic field of T1. The primary current of T1 is monitored through current transformer T2 and fed back to the pulse-width modulator as the timing ramp. This timing ramp is compared to the error voltage from either the constant voltage or the constant current control loop, and is also compared to a maximum primary current limit. When the primary current exceeds the lowest of these error voltages, the pulse-width modulator turns off the FETs, interrupting the primary current of transformer T1. The voltage across T1 reverses polarity as a result of the collapsing magnetic field and forces diode D3 to conduct, transferring energy through the output filter to the load. Error amplifiers U2 and U3 maintain either constant voltage or constant current operation by regulating the pulse width of the converter.

The use of the magnetizing current of T1 as the timing ramp for the pulse-width modulator improves the stability of the control loops. It also provides a convenient method of setting both a static and a dynamic limit on how much primary current will be allowed. This translates to defining the maximum output boundary as well as limiting the peak current in each of the power switches Q1 and Q2.

Power FETs

The use of power FETs for switches Q1 and Q2 provides many technical benefits that translate into customer features. For one, the turn-on and turn-off response of the FETs can be made quite rapid by driver circuit design, allowing operation at very small pulse widths (<100 ns), which occur at low output power (light load). This is particularly advantageous in a laboratory supply where bizarre behavior at light loading is undesirable.

In switching rapidly the power FETs dissipate almost an order of magnitude less power in switching loss than a bipolar transistor of similar ratings. In addition, the switching speed can be controlled from the gate, allowing EMI and switching loss to be easily predicted and controlled. The FETs exhibit no secondary breakdown phenomenon, thereby eliminating the need for snubber networks and their power dissipation. The FETs require insignificant static drive power and require energy supplied to the gate only during switching transistions. Therefore, the drive circuits can be simple, efficient, and reliable.

Another aspect of power MOSFETs is that they parallel

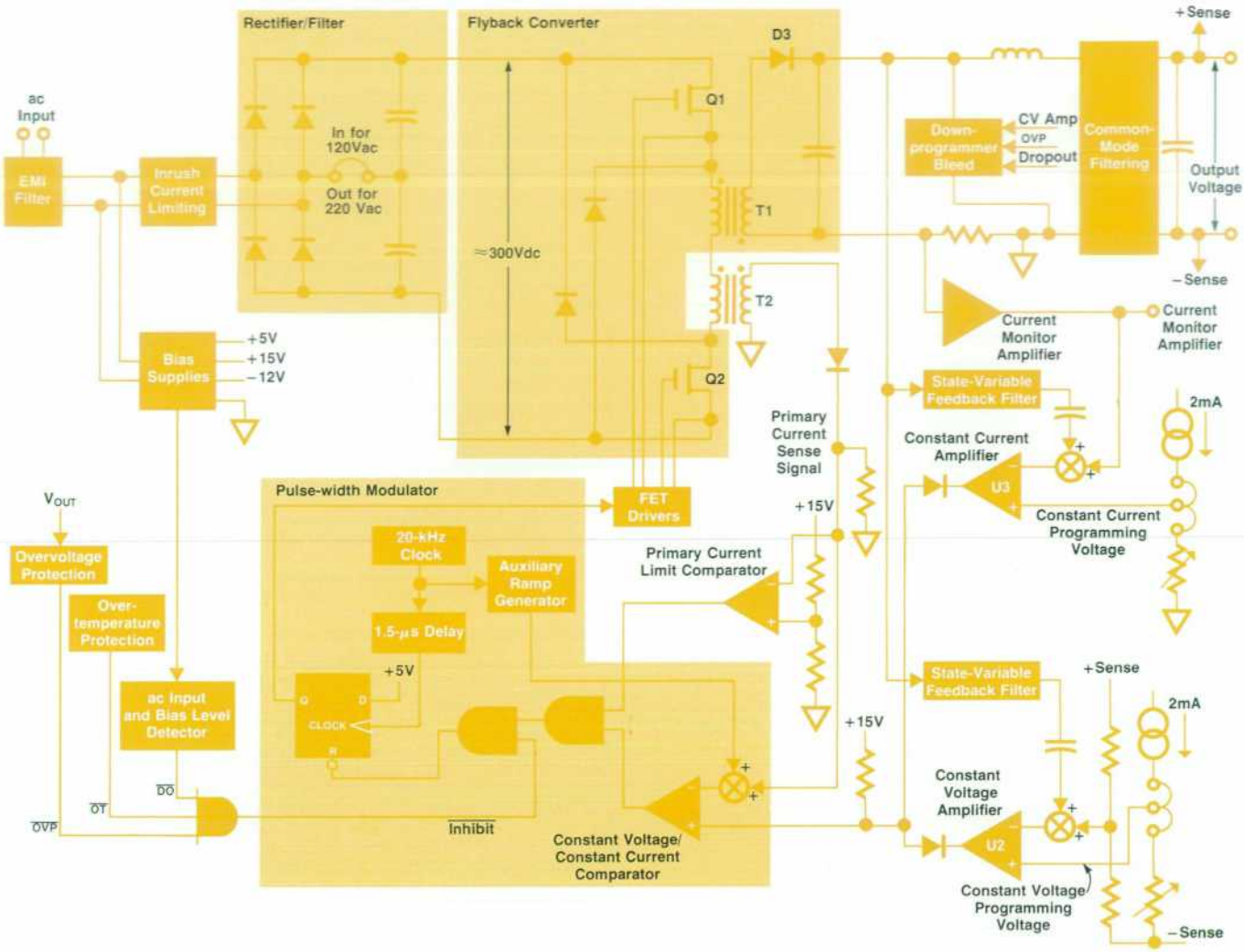


Fig. 4. *6012A/6024A block diagram. The design is a flyback converter using power metal-oxide-semiconductor field-effect transistors (MOSFETs) as switches.*

with great simplicity, sharing current equally, thanks to two mechanisms. Static current sharing is aided by the positive temperature coefficient of the FETs' on resistance, $R_{ds}(on)$.[1] Dynamic current sharing during switching is provided by small but roughly equal lead inductances in each source lead of the circuit. Reliable paralleling contributes substantially to the feasibility of a 1000-watt off-line laboratory-performance power supply.

Control Circuits

Since the converter tranfers energy on a cycle-per-cycle basis, power flow to the output can be halted by simply preventing clock pulses from reaching the pulse-width modulator. Circuitry that senses either insufficient bias voltage or dropout of the power line causes the clock pulses to be disabled, preventing energy transfer between the primary and the output. Should the internal thermostats sense unusually high temperature on the power components, clock pulses are again disabled and the converter has zero output. Should the output voltage exceed a customer-preset level, the overvoltage protection circuitry disables the clock pulses, again cutting off the output power.

The 6024A and 6012A are designed to operate over a wide range of loads. It was a significant design challenge to stabilize the control loops over their output operating ranges and with reactive loads. State-variable feedback techniques were employed to guarantee stability.

Minimum Output Operation

One problem that arises when applying pulse-width-modulated switching converters to laboratory power supplies is that inherent delays in control circuits and power switch devices may require that a certain minimum output power be dissipated for proper operation. In fixed-output supplies, this requirement is often satisfied by adding a load resistor to the supply to dissipate the minimum power. The main disadvantage of this approach is that this power is wasted.

In variable-output supplies, however, the problem becomes much more serious since it is very difficult to dissipate the power at zero output voltage. If the required power is dissipated by a resistor or an electronic load circuit at some low output voltage, the power dissipated at high output voltages becomes excessive. This is a particularly

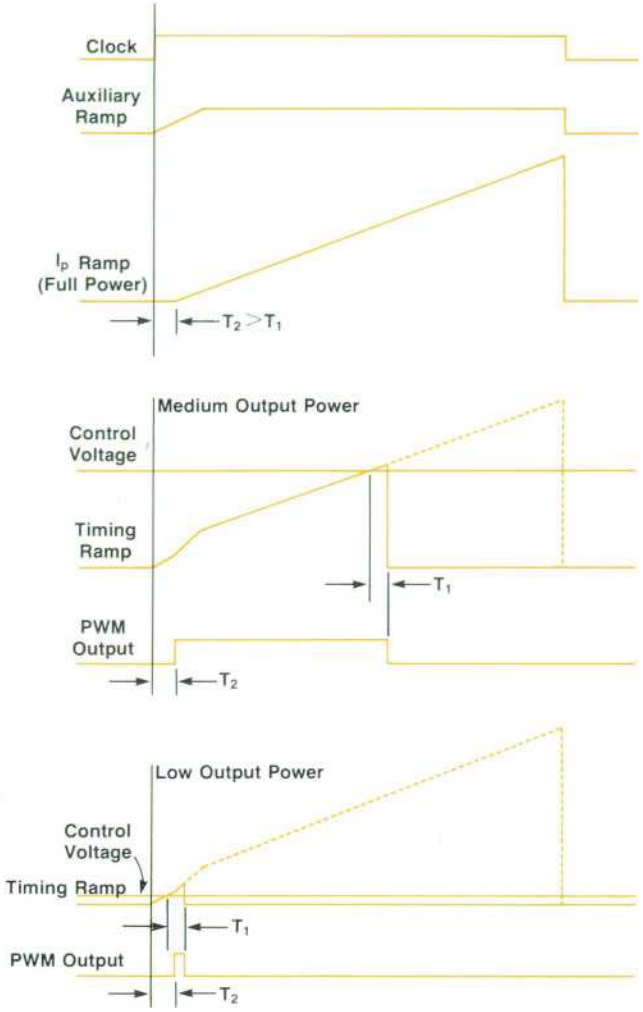


Fig. 5. *An auxiliary timing ramp added to the primary timing ramp takes effect at low output power so that very narrow, yet controlled pulse widths are produced by the pulse-width modulator (PWM) that switches the MOSFETs on and off. This allows efficient operation at combinations of low output voltage and current.*

nasty problem for autoranging supplies that experience large variations in output voltage.

Therefore, it was an important goal in the 6024A and 6012A to employ control circuit techniques and power devices that would allow the generation of very narrow, yet controlled pulse widths in the power converter, so that operation at combinations of low output voltage and current could be obtained with no output bleed.

The method employed to control the on time of the power FETs is to turn on the pulse-width modulator at the beginning of every clock cycle and turn it off when a timing ramp exceeds a control voltage. The timing ramp is a voltage signal that is proportional to the converter primary current, and the control voltage is the error voltage from the control loops.

Any delay (T_1) from the time when the timing ramp exceeds the control voltage to when the power switch turns off causes the primary current to increase beyond the desired value and transfer more energy to the output than required. For moderate and high output power, the control loops sense this condition and react by lowering the control voltage until the required on time is achieved. However, for low output power, this correction cannot occur, since the on time cannot be less than the value of the delay (T_1).

The delay consists of contributions from the comparator used to compare the ramp with the control voltage, the pulse-width modulator circuits, the power switch driver circuits, and the turn-off delay of the power switch itself. This delay is minimized by using high-speed comparators, pulse-width modulator logic, and driver circuits. In addition, the use of power MOSFETs rather than bipolar transistors significantly reduces the turn-off delay of the power switch. These steps reduce the effect of the delay, but do not eliminate it.

To make it possible to control the on time even when it is very small or zero, an auxiliary ramp is derived from the clock circuit and added to the primary current timing ramp. Two key features of this auxiliary ramp are that it starts at least T_1 earlier than the time the clock turns on the pulse-width modulator, and that its amplitude is limited to a low value to restrict its operation to small on times (see Fig. 5).

For large on times, the auxiliary ramp does not significantly affect circuit operation. However, for very small on times, the pulse timing is determined entirely by the auxiliary ramp. For very low values of control voltage, the auxiliary ramp can exceed the control voltage and start the turn-off process *before* the clock turns on the pulse-width modulator. In this way, the pulse-width modulator can produce very narrow pulses in the power converter and eliminate the need for a minimum output bleed.

Downprogrammer

The 6024A and 6012A are expected to be used as stimulus sources in many automatic test and industrial processes. Throughput is quite important in most of these applications. Accordingly, particular attention was given to the programming speed of these supplies.

The problem of rapidly decreasing the output voltage is accentuated by the fact that these are laboratory switching supplies. To meet the fairly stringent output noise specifications requires a great deal of filtering, resulting in a large capacitance across the output terminals, up to 10,000 μF in the 6012A. To change the capacitor voltage rapidly implies a considerable amount of available charging and discharging current. The charging current for up-programming is quite naturally available from the power mesh itself. However, other than the external load, which is unpredictable, there is no inherently available source of appreciable discharge current for downprogramming. Special circuitry had to be employed to meet the programming speed objectives.

To achieve rapid downprogramming, a power transistor actively discharges the output capacitor. The discharge current is made a function of output voltage to take full advantage of the transistor's safe operating area and to ensure protection from secondary breakdown. The circuit pulls increasingly more current at lower output voltages, giving the downprogrammer circuit an overall negative resistance characteristic (see Fig. 6). This circuit implementation achieves faster downprogramming than a constant-

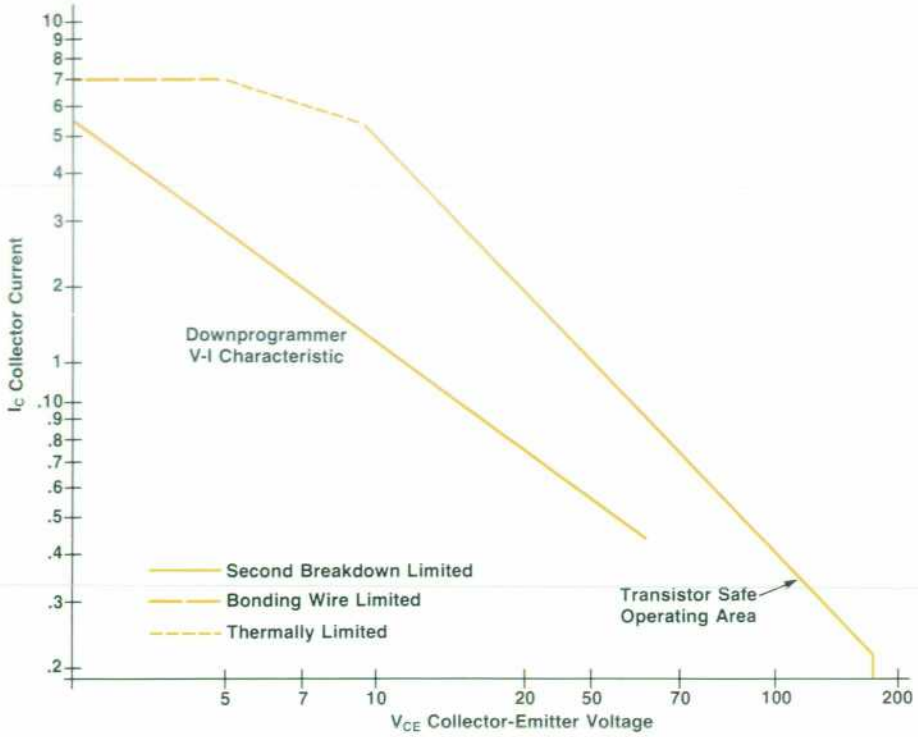


Fig. 6. *A downprogrammer with this negative resistance characteristic makes it possible to decrease the output voltage rapidly in automatic test and industrial process control applications.*

current or resistive load would, and results in the unusual downprogramming response characteristic shown in Fig. 7. In normal operation the downprogrammer circuit is disabled, so the negative resistance characteristic is not included in the feedback loop.

Systems Interface

Option 002 provides a convenient means for systems integration of either the 6024A or the 6012A by means of a 37-pin rear connector (see Fig. 8).

Six digital output lines that represent power supply status are optically isolated for connection to the customer's data inputs. The lines indicate constant voltage operation, constant current operation, power supply unregulated, overvoltage protection circuit tripped, overtemperature condition, and ac power dropout. Three digital input lines are also optically isolated. These trip the overvoltage circuit, clear the overvoltage circuitry, and provide for remote shutdown. +5, +15, and −15-volt bias supplies referenced to the power supply's bias circuit common are also provided. These bias supplies are particularly useful if the user wants to maintain electrical isolation between the power supply output and a controller. They can be used to power external circuitry such as D-to-A converters that must be referred to the power supply output.

Amplifiers are also provided to allow for current programming of the constant voltage and constant current channels, and for voltage and resistance programming of both channels. Monitor outputs provide 0-5 volts for zero to full-scale output voltage and output current.

By using the 6940B or 6942A Multiprogrammer and standard cards along with Option 002, systems integration of the 6024A and 6012A can be accomplished in minimal time. This can be a very attractive solution where the multiprogrammer (an I/O extender) is already necessary to automate an industrial process. Another advantage of this approach for large systems is that it allows control of multiple power supplies through a single I/O port of the controller.

Acknowledgments

Ken Woolley, Mike Mercadante, Rick DeRick, and Brian Swarts contributed to the design of the 6024A and Siu Wong, Rich Hilaire, Bill Emmons, and Bob Miller contributed to the design of the 6012A. However, the development was a team effort with close cooperation between both project groups. There are many other people not credited here who contributed to the products' success, and we hope it will suffice to say thanks to those not mentioned.

Reference

1. D. Gyma, J. Hyde, and D. Schwartz, "The Power MOSFET as a Switch, from a Circuit Designer's Perspective," Proceedings of Powercon 7, Power Concepts, Inc., Ventura, California, 1980.

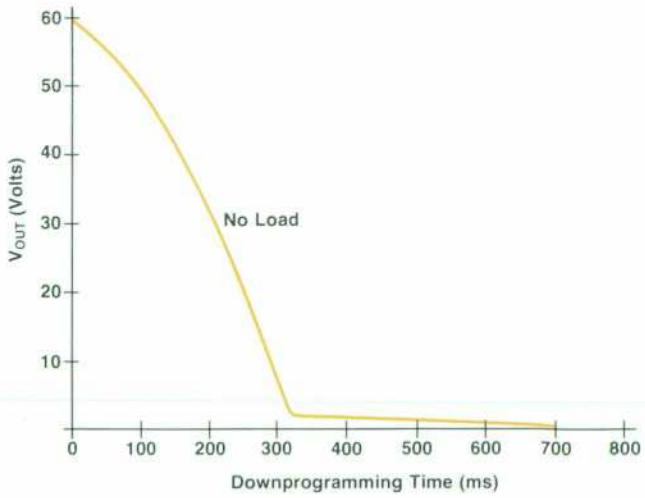


Fig. 7. *Model 6024A no-load downprogramming response.*

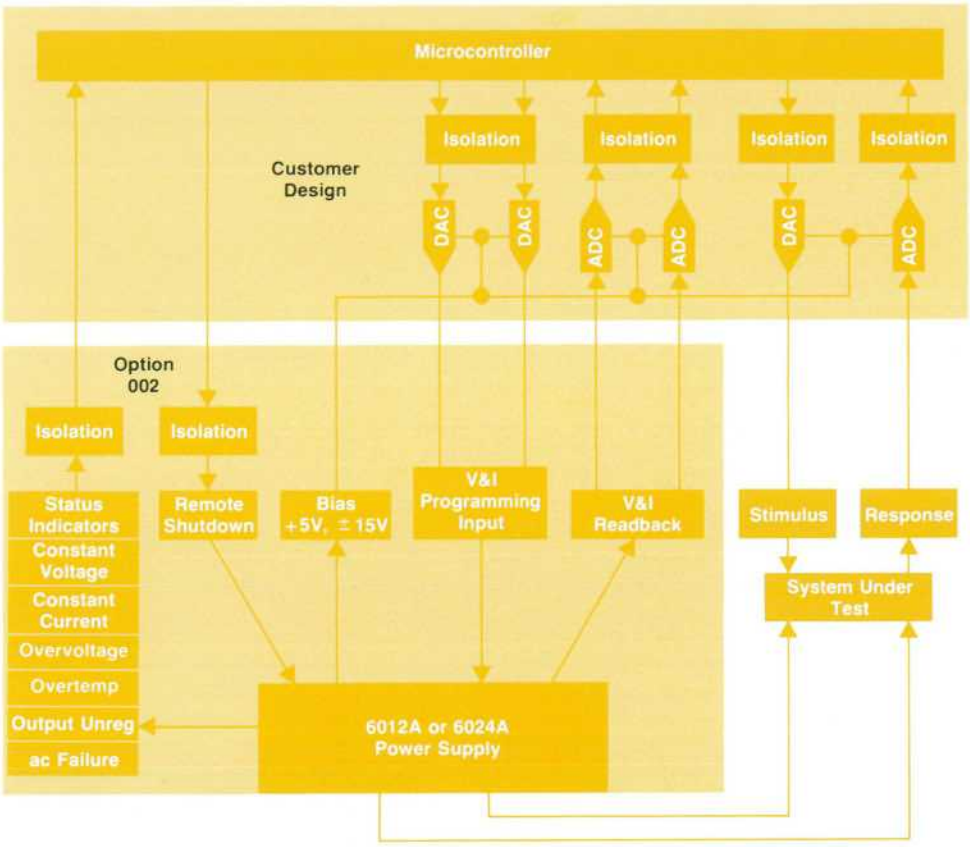


Fig. 8. *Option 002 provides a convenient 37-pin rear connector for systems integration of the 6012A or 6024A.*

Paul W. Bailey

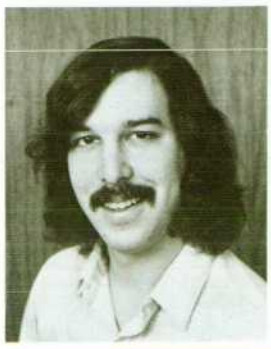
Paul Bailey joined HP's New Jersey Division in 1974 as a development engineer. He's served as project leader for the 6002A and 6024A Power Supplies, as project manager for laboratory and systems power sources, and as section manager for modular power supply development. His work has resulted in a patent on the downprogrammer circuit used in the 6012A and 6024A. Born in Possum Trot, Kentucky, Paul received his BSEE degree in 1973 from Massachusetts Institute of Technology and his MSEE degree in 1974 from the University of California at Berkeley. Paul is married, enjoys gardening and canning, likes to play basketball and watch Kentucky teams, and spends a good deal of time improving his home in Flanders, New Jersey.

John W. Hyde

John Hyde was born in Somerville, New Jersey and attended Rutgers University, graduating with BSEE and MSEE degrees in 1973 and 1975. He joined HP in 1975 and contributed to the electrical design of the 6002A and 6024A Power Supplies. Co-author of a paper on using power MOSFETs as switches, he's now a project leader with HP's New Jersey Division. John lives in Parsippany, New Jersey, and enjoys photography, guitar, and gardening.

Dennis W. Gyma

Dennis Gyma was project leader for the 6012A Power Supply and is now laboratory and industrial section manager with HP's New Jersey Division. A native of Newark, New Jersey, he received his BSEE and MSEE degrees from Rutgers University in 1973 and 1975. With HP since 1975, he's co-author of a paper on using power MOSFETs as switches. Dennis is married, has a son, and lives in Netcong, New Jersey. He's an accomplished acoustic and electric guitarist, and he enjoys gardening.



Daniel R. Schwartz

Dan Schwartz received his BE degree from Cooper Union in 1976 and his MSE degree from Princeton University in 1977. He joined HP in 1977, contributed to the design of the 6012A Power Supply, and is now a project leader with HP's New Jersey Division. A member of IEEE, he's co-author of a paper on using power MOSFETs as switches. A resident of Irvington, New Jersey, Dan enjoys basketball, audio, recording live performances, and spending time in his native New York City.

SPECIFICATIONS

HP 65000A Series 50W Power Supplies

HP Model Number	Outputs* Name	Nominal Voltage (Vdc)	Maximum Current (Adc)	Typical 50W Application (Adc)	Size L×W×H (mm)	Weight (gm)
Single Output						
65105A	V1	5	10.0	10.0	180×127×38	454
65112A	V1	12	4.2	4.2		
65115A	V1	15	3.3	3.3		
Single +2 Outputs						
65312A	V1	5	10.0	5.0		
	V2	+12	1.5	1.0		
	V3	−12	1.5	1.0		
65315A	V1	5	10.0	5.0	218×127×38	510
	V2	+15	1.0	0.8		
	V3	−15	1.0	0.8		
65317A	V1	5	10.0	5.0		
	V2	+18	1.0	0.7		
	V3	−18	1.0	0.7		
Triple +2 Outputs						
65512A	V1	5	10.0	5.0	264×127×43	624
	V2	+16	1.0	0.4		
	V3	−16	1.0	0.4		
	V4	+5 to +12	0.3 to 1.0	0.5 @ +12		
	V5	−5 to −12	0.3 to 10	0.5 @ −12		
Quadruple +2 Outputs						
65612A	V1	5	10.0	4.0	264×127×43	624
	V2	+16	1.0	0.7		
	V3	−16	1.0	0.6		
	V4	−5 to +12	0.3 to 1.0	0.3 @ −12		
	V5	−5 to +12	0.3 to 1.0	0.3 @ −12		
	V6	−5 to −12	0.3 to 1.0	0.1 @ −5		

*V1 is the Main Output. V2 and V3 are semi-regulated extra outputs. V4, V5, and V6 are adjustable over the range given.

INPUT VOLTAGE: 87-127Vac/174-250Vac, 47-63 Hz
TEMPERATURE OPERATING: 0-50°C convection cooled
0-70°C fan cooled
STORAGE: −20 to 85°C
CARRYOVER TIME: 25 ms minimum at 115 or 230Vac
10 ms minimum at 104 or 208Vac
EFFICIENCY: 70 to 76% typical
REMOTE SHUTDOWN: Latching shutdown via TTL pulse
REMOTE SENSE: V1 only, ±5% range.
OUTPUT DRIFT: 0.25% maximum 8 hrs after 1-hour warmup
OVERTEMPERATURE: 80±5°C automatic shutdown
SAFETY RECOGNITIONS: UL478, UL114, CSA 22.2/143 and CSA 22.2/154
SAFETY DESIGN TO: VDE 0730/2P and IEC348
EMI: VDE 0871 Class B with external cover and filter
OVERCURRENT PROTECTION: All outputs protected, V1 and V4-V6 thermally protected, V2-V3 fused.
OVERVOLTAGE PROTECTION: V1 and V4-V6 automatic shutdown, V2-V3 voltage clamped.
OTHER OUTPUT SPECIFICATIONS (WORST OF ALL MODELS)

Output	REGULATION Line %	Load %	Cross %	PARD mV_{p-p}	TEMP COEF Max %/°C
V1	0.1	0.1	0	150	.02
V2, V3	5.0	12.0	7	200	.10
V4-V6	2.0	2.0	0	200	.10

PRICES IN U.S.A.:

	Unit	1000 qty.
Single Output	$195	$154
Single + 2 Outputs	$240	$190
Triple + 2 Outputs	$255	$201
Quadruple + 2 Outputs	$265	$209

HP Model 6024A Power Supply - 200W

DC OUTPUT: Voltage and current output can be adjusted over the range indicated by using front-panel controls, analog programming, or optional system interface.
VOLTAGE: 0-60V CURRENT: 0-10A
Maximum available output power from 20V to 60V is indicated in Fig. 3 on page 12.
LOAD EFFECT: (Load Regulation):
VOLTAGE: 0.01% + 3 mV CURRENT: 0.01% + 3 mA
SOURCE EFFECT:
VOLTAGE: 0.01% + 2 mV CURRENT: 0.01% + 2 mA
PARD (Ripple and Noise) rms/p-p. 20 Hz to 20 MHz:
VOLTAGE: 3 mV/30 mV CURRENT: 5 mA rms
TEMPERATURE COEFFICIENT: Δ/°C after 30-minute warmup:
VOLTAGE: 0.01% + 1 mV CURRENT: 0.03% + 1 mV
DRIFT: (Stability) change in output over an 8-hour interval.
VOLTAGE: 0.03% + 3 mV CURRENT: 0.03% + 3 mV
REMOTE CONTROL (ANALOG PROGRAMMING):
Resistance necessary for full-scale output of:
VOLTAGE: 2500Ω CURRENT: 2500Ω
ACCURACY: 0.8% + 1 mV ACCURACY: 2.4% + 1 mA
Voltage necessary for full-scale output of:
VOLTAGE: 5 volts CURRENT: 5 volts
ACCURACY: 0.2% + mV ACCURACY: 0.9% + 1 mA
PROGRAMMING RESPONSE TIME: Maximum time for output voltage to change from 0V to 60V or 60V to 2V and settle within 60 mV.
UP: Full Load (18Ω) 200 ms DOWN: Full Load (18Ω) 300 ms
No Load 200 ms No Load 600 ms
OVERVOLTAGE PROTECTION: Trip voltage adjustable from 2 to 64 volts.
AMPLIFIED CURRENT MONITOR: 0-5V monitor output for 0-10A output.
EMI SPECIFICATIONS: Meets VDE 0871/6.78 Level A.
SAFETY SPECIFICATIONS: Complies with IEC 348, VDE 0411, CSA 556B, CSA C22.2 #0-1975.
TEMPERATURE: OPERATING: 0 to 55°C.
STORAGE: −40 to +75°C.
AC INPUT: 104-127Vac 48-63 Hz, 5.3A rms maximum.
WEIGHT: Net 5.4 kg (12 lb). Shipping 7.3 kg (16 lb).
SYSTEM INTERFACE OPTION: Same as system interface option for 6012A except voltage accuracy is 0.3% + 7 mV and current accuracy is 1% + 2 mA.
PRICES IN U.S.A.:
6024A Power Supply, $875.
Option 002: System Interface, $300.
Option 100: 87-106Vac, 48-63 Hz, N/C. (Output derated to 50V, 150W.)
Option 220: 191-233Vac, 48-63 Hz, N/C.
Option 240: 208-250Vac, 48-63 Hz, N/C.

HP Model 6012A Power Supply - 1000W

DC OUTPUT: Voltage and current output can be adjusted over the range indicated by using front-panel controls, analog programming, or optional system interface.
VOLTAGE: 0-60V CURRENT: 0-50A
Maximum available output power from 20V to 60V is indicated in Fig. 3 on page 12.
LOAD EFFECT: (Load Regulation):
VOLTAGE: 0.01% + 5 mV CURRENT: 0.01% + 5 mA
SOURCE EFFECT:
VOLTAGE: 0.01% + 3 mV CURRENT: 0.01% + 5 mA
PARD (Ripple and Noise) rms/p-p. 20 Hz to 20 MHz:
VOLTAGE: 5 mV/50 mV CURRENT: 25 mA rms
TEMPERATURE COEFFICIENT: Δ/°C after 30-minute warmup:
VOLTAGE: 0.01% + 2 mV CURRENT: 0.01% + 3 mA
DRIFT: (Stability) change in output over an 8-hour interval.
VOLTAGE: 0.03% + 5 mV CURRENT: 0.03% + 5 mA
REMOTE CONTROL (ANALOG PROGRAMMING):
Resistance necessary for full scale output of:
VOLTAGE: 2500Ω CURRENT: 2500Ω
ACCURACY: 1% + 3 mV ACCURACY: 2.5% + 10 mA
Voltage necessary for full-scale output of:
VOLTAGE: 5 volts CURRENT: 5 volts
ACCURACY: 0.3% + 3mV ACCURACY: 1% + 10 mA
PROGRAMMING RESPONSE TIME: Maximum time for output voltage to change from 0V to 60V or 60V to 2V and settle within 200 mV.
UP: Full Load (3.4Ω) 120 ms DOWN: Full Load (3.4Ω) 400 ms
No Load 120 ms No Load 1.2 s
OVERVOLTAGE PROTECTION: Trip voltage adjustable from 2 to 60 volts.
AMPLIFIED CURRENT MONITOR: 0-5V monitor output for 0-50A output.
EMI SPECIFICATIONS: Meets VDE 0871/6.78 Level A.
SAFETY SPECIFICATIONS: Complies with IEC 348, VDE 0411, CSA 556B, CSA C22.2 #0-1975.
TEMPERATURE: OPERATING: 0 to 50°C.
STORAGE: −40 to +75°C.
AC INPUT: 104-127Vac 48-63 Hz, 24A rms maximum.
WEIGHT: Net 15 kg (33 lb). Shipping 16 kg (35 lb).
SYSTEM INTERFACE OPTION REMOTE CONTROL (ANALOG PROGRAMMING):
Sink current necessary for full scale of:
VOLTAGE: 2 mA CURRENT: 2 mA
ACCURACY: 0.4% + 9 mV ACCURACY: 1.1% + 15 mA
ISOLATION: Status and control lines; 600Vdc max from equipment ground, from the power supply output or from each other.
PRICES IN U.S.A.:
6012A Power Supply, $1550.
Option 002: System Interface, $300.
Option 100: 90-105Vac, 48-63 Hz, N/C. (Output derated to 50V, 750W.)
Option 220: 191-233Vac, 48-63 Hz, N/C.
Option 240: 208-250Vac, 48-63 Hz, N/C.
MANUFACTURING DIVISION: NEW JERSEY DIVISION
Green Pond Road
Rockaway, New Jersey 07866 U.S.A.

The Vertical Power MOSFET for High-Speed Power Control

A vertical semiconductor device structure provides a power MOSFET that can switch high currents and voltages very rapidly. This makes it useful for power supplies, pulse drivers, and switching amplifiers.

by Karl H. Tiefert, Dah Wen Tsang, Robert L. Myers, and Victor Li

POWER AND FREQUENCY are natural electronic enemies. In a variety of detailed technical ways, as well as in fundamental ones, the speed of operation of a device is limited by its operating power level. As new technology is developed, old speed and/or power barriers are overcome and new limits are established, as described qualitatively in Fig. 1.

A new component development leading to a major shift in power-frequency performance is the vertical power MOSFET (metal-oxide-semiconductor field-effect transistor). In this device, the best features of earlier technologies and innovative device design are combined with state-of-the-art MOS wafer fabrication techniques to achieve performance that in some applications can be an order of magnitude better than that previously attainable.

Semiconductor Power Switches

Designers and manufacturers of power conversion and control equipment are constantly seeking a more efficient switch. This is because the efficiency of controlling or converting electrical power using modern pulse modulation techniques as illustrated in Fig. 2 is directly related to the efficiency of the switch. A source of dc power (usually rectified ac line voltage) is modulated by the switch to regulate the amount of power supplied to the load. Output voltage is sensed at the load by the control circuit which in turn feeds a control signal back to the pulse modulator. The pulse modulator controls the amount of power delivered to the load by varying the switch's duty cycle by either pulse-width or repetition-rate modulation. An energy analysis of this system provides a definition of an ideal switch against which devices can be measured. To have zero power consumption, an ideal switch has zero resistance in the on state and zero current leakage in the off state, and makes the transition between these states in zero time. The ideal switch also requires zero drive power and is capable of unlimited repetition rates. The latter feature allows reduction of magnetic and filter component sizes. As switch characteristics approach ideal values, power control and conversion equipment can be made more efficient, smaller, and usually less expensive.

Until recently, conventional solutions to the problem of providing industry with an ideal switch (or at least a practical one) have been realized in the form of thyristors, bipolar transistors, and planar field-effect transistors. Each of these devices has advantages and limitations.

The thyristor (SCR, triac, etc.) is a bistable solid-state device that blocks the flow of current until turned on by a

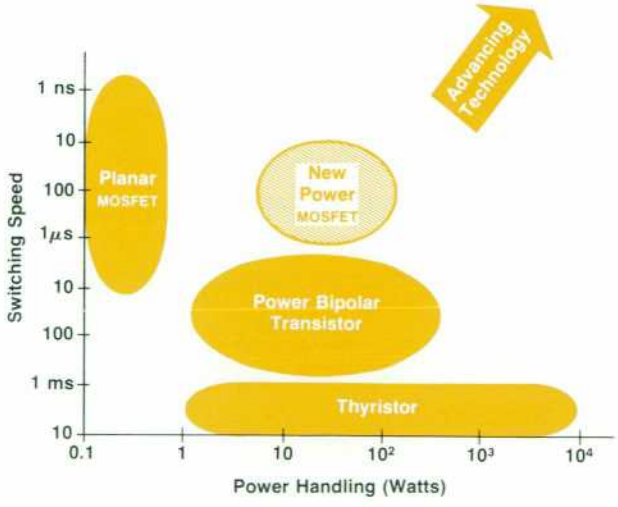


Fig. 1. *Speed versus power for various power semiconductor devices. Technology advances are generally upward to the right.*

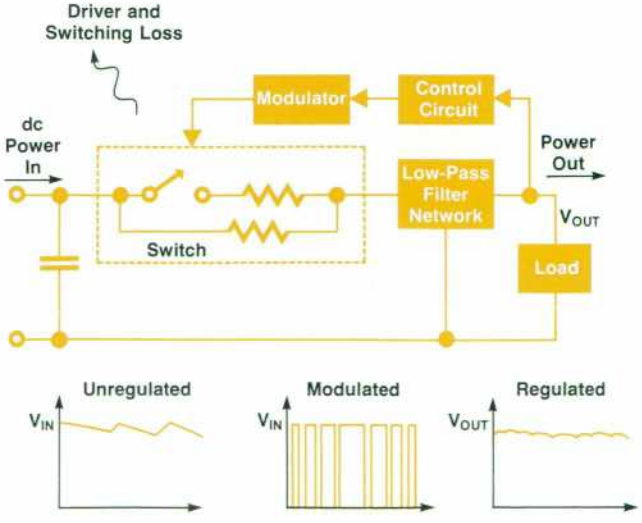


Fig. 2. *A block diagram of a basic power controller using an ideal switching element.*

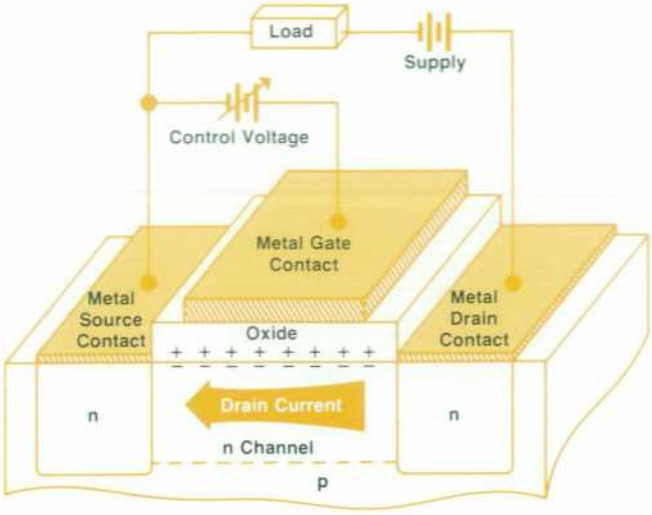


Fig. 3. *Simplified cross section of a planar MOSFET. Current flows laterally from the drain under the gate to the source.*

small control signal. Once turned on, the thyristor remains on until the supply voltage is removed or reversed in polarity. While these devices are able to control large amounts of power (up to hundreds of kilowatts), they are usually limited to switching frequencies of only a few kilohertz. The speed limitation and inability to be turned off by a control signal severely limits their general application to direct control of power to a load from the ac power line. Common applications are motor speed controllers and light dimmers.

The workhorse of the power control industry has been the bipolar power transistor. This ubiquitous device has been used for almost every conceivable power control application from servo controls to switched-mode amplifiers. The bipolar power transistor functions in the same way as its small-signal counterpart, but is physically larger to enable it to handle power levels up to several hundred watts. The bipolar power transistor is a current amplifying device with low dc power gain. A continuous base current is required to maintain this device in the on state. This base drive power is lost and detracts from the bipolar transistor's efficiency as a switch. Although it is capable of switching at a much higher rate than the thyristor, time delays associated with switching loss and the injection and removal of base charge limits practical switching rates to less than 20 kHz. The bipolar

Fig. 4. *The HP Model HPWR-6501-Series Power MOSFETs are mounted in TO-3 packages as shown. Units are 100% tested before shipment.*

Power MOSFET Performance Useful for Many Applications

The vertical power MOSFET combines the circuit advantages of planar FETs with the surface packing density of vertical device structures to offer efficient and convenient control of high currents and voltages. Because of its exceptional switching speed as a majority carrier device, it can be operated at far higher switching rates than any of the alternative devices at equivalent power levels. The applications that can benefit from this additional performance are:

- Switching power supplies. The fast switching speed of the power MOSFET reduces switching losses in switching power supplies by reducing the period of time during which significant voltage and current occur simultaneously at the device terminals. This speed allows higher repetition rates that can be used to reduce the size of transformers and filter elements, thereby reducing size, weight and cost of associated power supply circuitry. The simplified drive requirement (capacitance as compared to base charge storage in the bipolar transistor, for example) results in simpler, less expensive drive circuits. Majority-carrier operation avoids negative resistance temperature coefficients and hence avoids thermal runaway, secondary breakdown, and other deleterious effects, while allowing devices to be paralleled without concern. These uncomplicated modes of operation lead to rugged performance. See the two articles on MOSFET switching power supplies in this issue for further details (pages 3 and 11).
- Pulse drivers. The power MOSFET pulse response is excellent. Transition speeds are in the nanosecond range for kilowatt power levels, and the absence of storage delays and other minority-carrier effects offers both pulse fidelity and device ruggedness. Straightforward input and output impedance makes pulse-circuit matching a relatively easy task.
- Switching amplifiers. Switching amplifiers provide analog gain by conversion of an input signal amplitude to pulse-width modulation, amplification of this pulse by an efficient switch, and subsequent demodulation to retrieve the analog amplitude. Class D amplifiers operate in this mode. This application can use most of the power switching features of the power MOSFET. Here, switching efficiency contributes directly to all the normal amplifier performance characteristics—gain, linearity, low distortion, power efficiency, and power-handling capability versus temperature. Switching speed and repetition rate, in particular, contribute directly to available bandwidth; hence power MOSFETs can offer a major extension of performance.
- Linear (analog) power amplifiers. For amplification and power, the usual figures of merit are gain-bandwidth product, power-frequency-squared product, low distortion, and dynamic range. The basic frequency capabilities of the power MOSFET and its square-law transfer behavior should enhance all of the high-frequency power parameters mentioned.

Specific information is available in Hewlett-Packard's application note AN-977 and application bulletins AB-32, 33, 34, and 35.

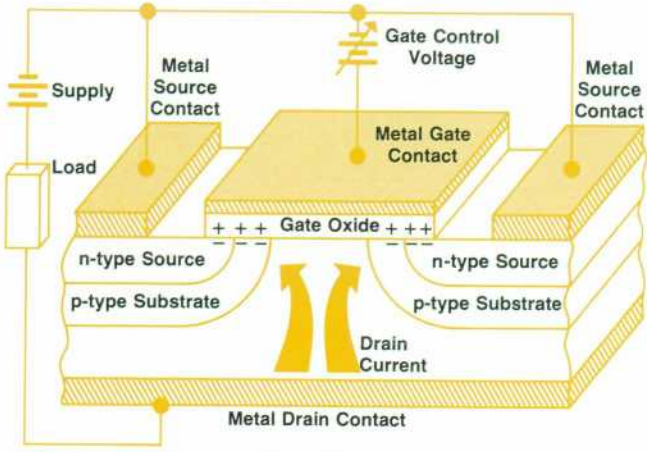


Fig. 5. *Simplified cross section of a vertical power MOSFET. The drain is located on the bottom and the source on top. Current flows upward under the gate and then outward to the source regions.*

power transistor also suffers from other disadvantages, such as potential thermal instability and secondary breakdown (a condition of destructive thermal runaway resulting from the simultaneous presence of high currents and high electric field), that restricts its ability to control power to a reactive load.

A third alternative is the planar MOSFET. This device comes very close to meeting two of the ideal switch's characteristics. As a voltage-controlled current device, an almost neglible amount of power is required to control the switching action of the MOSFET. Also, lacking the time delays inherent in a bipolar junction device, the planar MOSFET can easily be operated at frequencies up to hundreds of megahertz. The operation of the planar MOSFET is shown in Fig. 3. The flow of current through the channel is controlled by an electric field that is generated by a voltage applied to the gate terminal. Since the gate is electrically insulated from the rest of the device, no dc current can flow to the gate and only a small amount of power is consumed in charging and discharging the gate capacitance during switching. Unfortunately, the current to be controlled is conducted laterally through a relatively long channel. This causes a significant voltage drop to appear between the drain and source terminals. The result is a high on resistance of 10 to 100 ohms, a large departure from our ideal switch. This high on resistance causes an appreciable power dissipation in the channel, thus limiting the use of the planar MOSFET as a switch to applications handling power of one watt or less.

Vertical Power MOSFET

Up to now, users of power semiconductors were faced with selecting either power or speed: take your choice. The thyristor, while able to handle kilowatts of power, is generally limited to line-frequency control of ac power. The planar MOSFET is amazingly fast, but can only control about one watt of power. As a compromise, the bipolar power transistor offers a moderate power capability at intermediate switching speeds.

Now, however, a new technology called vertical DMOS (double-diffused MOS) has combined bipolar power and MOSFET speed into one device. This device, the HP Model HPWR-6501-Series Power MOSFET (Fig. 4), has made the design of low-cost, reliable, and efficient power supplies possible (see article on page 3). Its basic operation is illustrated in Fig. 5. In contrast to the surface conduction path in the planar MOSFET, current flows vertically through the vertical DMOS device. This allows drain current to be collected from the device substrate, removes the need to allow for drain contact area on the surface of the device, and in effect doubles the active gate area on the chip. Such increases in packing density directly reduce the cost and improve the performance of the device. Like the planar MOSFET, the flow of drain current is controlled by a voltage applied to the gate terminal. A positive gate voltage causes a conductive channel to be induced in the p-type* material immediately under the gate oxide layer. This channel allows a controlled amount of current to be conducted from the drain to the source terminal. A vertical power MOSFET actually consists of thousands of these basic cells connected in parallel on a single chip of silicon.

How It Works

A simplified cross-section drawing illustrating some of the principal elements of a Hewlett-Packard power MOSFET is shown in Fig. 6. The gated channels are to the left; the edge of the device is to the right. In the active region, an n-channel DMOS structure is used. The channel is defined by two consecutive thermal diffusion processes rather than

*Editor's Note: Throughout this discussion reference is made to various impurity (doping) concentrations by using the designations p−, p, p+, n−, n, and n+. Acceptor impurities are indicated by p and donor impurities by n. Lightly doped (concentrations less than 10^{15} atoms/cm^3) regions are indicated by the minus sign and heavily doped (concentrations greater than 10^{19} atoms/cm^3) areas by the positive sign.

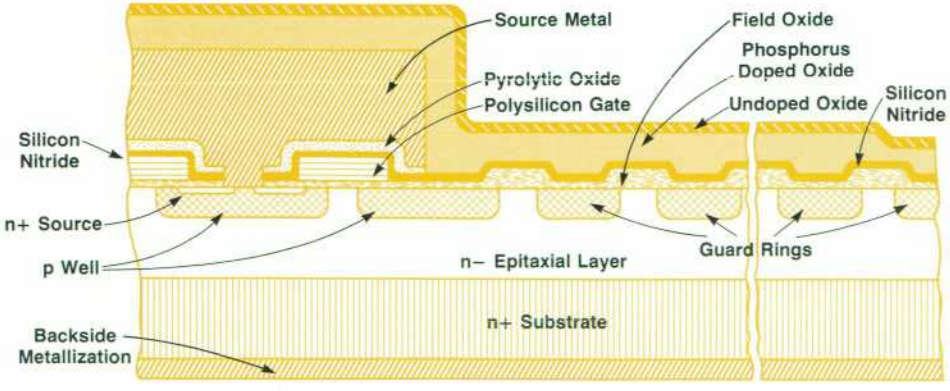


Fig. 6. *Cross section of the HP vertical power MOSFET showing the guard-ring structure on the right. This structure distributes the electric fields at and near the top surface to maintain a high voltage breakdown capability.*

by photolithography, thereby producing a very well controlled and very narrow channel length. The diffused channel has a graded impurity (doping) concentration that prevents punchthrough voltage breakdown when a large drain-to-source voltage is applied. The short channel length reduces transit time and gives the DMOS device the high speed necessary for a fast switch. A full surface metallization contacts both the n+ source region and the p-well on the top surface. Polycrystalline silicon is used for the gate electrode, which is insulated from the source metal by a sandwich structure of pyrogenic silicon dioxide, silicon nitride, and pyrolytic silicon dioxide layers and contacted at various places by the gate connection metal. The drain region is an n− epitaxial (epi) layer grown on an n+ substrate. The substrate is contacted on the bottom surface by backside metal to form the ohmic contact. Current in the device flows laterally through the channel region and then vertically down through the epi layer.

Because of the presence of high electric fields near and at the surface, the periphery of the device must be protected against premature breakdown. This is done in the HP power MOSFET by adding specially designed guard rings as shown in Fig. 6. These guard rings function as voltage dividers to distribute the high voltage, which would otherwise appear only across the main pn junction. This reduces the maximum field strength at the surface and at the diffused cylindrical pn junctions.

Since conduction is by majority carriers in these devices, charge storage delay is insignificant compared to that for bipolar transistors. Under normal operating temperatures, current crowding and local hot spots do not occur because the thermal coefficient of resistivity is positive. Thus, the secondary breakdown phenomenon encountered in bipolar transistors is eliminated.

The vertical DMOS FET greatly improves the device packing density per unit area which results in other advantages such as high-current handling capability and high transconductance. Some typical electrical characteristics for an HP device packaged in a TO-3 package are given in the specifications on page 23. The maximum current rating is determined to a large extent by packaging limitations and not by the device.

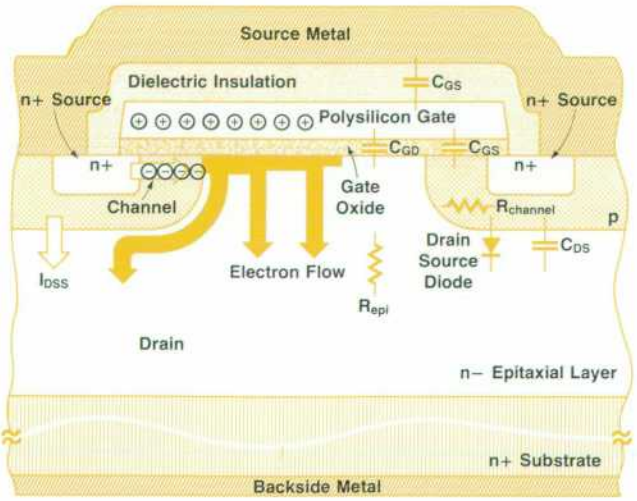


Fig. 7. *Cross-section of a single cell of the vertical power MOSFET showing electron flow and parasitic elements.*

Principles of Operation

As the name MOSFET suggests, the flow of current is controlled by an electric field. To illustrate this, let us look at Fig. 7 which is an enlargement of a single cell of the device structure shown in Fig. 6. Notice that, with the vertical arrangement, a polysilicon gate has two channel regions. The width of the polysilicon gate and the associated spacing between the two p wells are chosen to maximize packing density and minimize resistance. This is very different from the lateral arrangement, which not only uses up one side of the gate for a drain contact, but also requires a wider polysilicon gate to withstand the full drain-to-source voltage. Besides these savings in device active area, the large topside surface area, which otherwise would be wasted on a drain bonding pad and drain metal interconnections, can now be used to create more channels when the drain terminal is moved to the bottom of the chip. The result is a very efficient design that, compared to a lateral structure with the same device area, more than doubles the transconductance and current handling capability while reducing the epitaxial-layer resistance by nearly half.

The formation of a conductive channel and electron flow is shown on the left-hand side of Fig. 7 while schematic circuit elements are indicated on the right. For normal operation, the drain-to-source voltage is positive. This places the pn drain-source diode in reverse bias, allowing only a minute reverse leakage current. However, if a conductive channel is created along the silicon surface beneath the gate oxide, a large current can flow in the direction indicated.

When the drain-to-source voltage is negative, the drain pn junction is forward biased through the p diffusion and the source contact. In this condition drain-to-source current is simply that of the large diode junction and is unaffected by the gate. This feature is used to limit negative voltage excursions in some applications.

In normal operation a conductive channel can be created if the proper gate bias is applied. A negative gate bias attracts positive charges toward the silicon surface. For zero or negative gate bias, we encounter two pn junctions as we travel from source to drain under the gate. If a positive drain-to-source bias is applied, both of these junctions will be reverse biased, no current can flow, and the device is off.

If, on the other hand, a positive gate bias is applied, negative charges will gather under the gate. From source to drain, we see a continuous concentration of free electrons which forms a conduit for charge flow. The pn junctions that acted as barriers under a negative gate bias no longer exist because the p region under the gate is now turned into a thin n-type layer. The application of a drain-to-source field (or voltage) causes drain-to-source current and the device is on.

The amount of current depends on the gate potential applied and the extent to which electrons are attracted toward the surface. When the drain-to-source potential is small, the gate electrode has the predominant influence in the channel region underneath it, current is linear with applied drain-to-source voltage and the larger the gate po-

tential, the lower the channel resistance will be. In MOSFET terminology, this mode of operation is termed the "linear region." The interplay of the various potentials and the net current that results are summarized in the following equation:

$$I_{DS} = \frac{W\mu\epsilon}{Lt_{ox}}\left[V_{DS}(V_{GS} - V_{GS}(th)) - \frac{(V_{DS})^2}{2}\right]$$

where W is the channel width, L is the channel length between drain and source, μ is the surface electron mobility, ϵ is the dielectric constant of the semiconductor material, and t_{ox} is the gate oxide thickness. V_{DS} and V_{GS} are drain and gate voltages respectively, both referenced to the source. The quantity $V_{GS}(th)$, (termed the threshold voltage, a complex quantity encompassing the substrate doping, the nature of the oxide, and the semiconductor oxide interface) provides a measure of the gate potential required to cause sufficient electrons to be attracted to the surface for current conduction. This quantity can be tailored to suit the designer's or user's need.

This seemingly complex expression is quite straightforward to derive. The key is to account for the number of electrons attracted to the p-well surface by the effective gate potential while treating the gate-oxide-channel system as a capacitor. Then the conductivity of the channel can be estimated. The charge flow resulting from a drain-to-source bias follows familiar textbook approaches used to calculate the conduction current inside a semiconductor.

As the drain-to-source potential is increased for a fixed gate voltage, the region in the channel close to the metallurgical pn junction will see increasingly less and less gate bias compared to the n+ source end. Eventually, a drain-to-source voltage is reached, which we label as V_{sat}, when the gate bias no longer attracts any electrons to the surface and a region devoid of both electrons and holes appears at the drain end of the channel. From this point any additional drain-to-source bias will appear across this high-resistance depletion layer rather than across the ohmic channel. The channel current therefore becomes fixed by the maximum voltage V_{sat} and ceases to rise with drain-to-source bias, and the saturation mode of operation is reached. The maximum channel current for a particular gate voltage in this mode is given by

$$I_{DS} = \frac{W\mu\epsilon}{2Lt_{ox}}(V_{sat})^2 \quad , \quad \text{where } V_{sat} = V_{GS} - V_{GS}(th)$$

The characteristic square-law dependence of drain-to-source current and the gate bias voltage is a prominent feature of this mode of operation.

Thus, there are three main regions of MOSFET operation: off, linear (or ohmic) region, and the saturation region. Notice that the terms linear and saturation refer to quite different physical phenomena from similar terms used for a bipolar device. The conventional circuit model and small-signal equivalent circuit for a MOSFET apply to the vertical power MOSFET to a large extent. These are given in Fig. 8 with some modifications.

How It Is Made

The double-diffused MOS (DMOS) process (Fig. 6) for vertical power MOSFETs uses a polysilicon gate technology combined with ion implantation and diffusion techniques that provide self-alignment of the gate areas. This process provides very high gate packing density which together with the large area of the devices results in low drain-to-source resistance (R_{DS}).

The devices are built on highly doped, low-resistivity n-type wafer substrates. The first process step is the deposition of a lightly doped epitaxial silicon layer. The thickness and doping level of this layer are determined by the desired breakdown voltage of the devices. This epitaxial deposition is followed by the growth of a silicon dioxide (SiO_2) layer that is photomasked and chemically etched to define the device areas and the guard ring structures.

After a thorough cleaning step the gate oxide is grown, followed immediately by the low-pressure chemical vapor deposition (LPCVD) of a polycrystalline silicon layer. Using photomasking and plasma etching techniques the gate lines are defined. Together with the photoresist, they are used in the next step to mask against the boron ion implant. The implantation of boron and the subsequent drive-in diffusion establish the p-well areas and the guard rings.

The next masking operation removes all SiO_2 from the devices except over the guard rings and portions of the areas where the source contacts are to be made. The following phosphorous source deposition and diffusion serve two purposes: to dope the polysilicon gate lines for better electrical conduction, and to create the n+ source areas.

The entire device area is then passivated with silicon nitride (Si_3N_4). To allow chemical etching of the Si_3N_4 layer an SiO_2 mask layer deposited by LPCVD is required. Using this mask the contact openings are etched into the Si_3N_4 and underlying SiO_2 layers. An aluminum-silicon (Al-Si) layer is deposited on the top surface of the wafer and then photomasked and etched such that all source contacts are connected via two metal plates and the contact areas of the gate lines are connected by means of interconnecting metal stripes. After low-temperature LPCVD of the SiO_2 scratch-protection layer, the last photomasking and etching step defines the bonding pad areas. The titanium-silver (Ti-Ag) metallization on the back of the wafer is then applied using planar magnetron sputter deposition.

After 100% dc testing, the wafers are sawed into individual chips. These are die-attached, wire-bonded and hermetically sealed into TO-3 packages to make up the final product. After process completion all finished devices are 100% tested before shipment and samples of each production run are subjected to a special reliability test program.

Positive and negative gate bias stressing at 200°C verifies

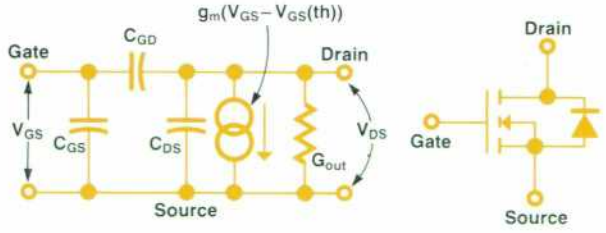


Fig. 8. *Small-signal equivalent circuit for the power MOSFET.*

the stability of the $V_{GS}(th)$ characteristics under high-temperature reverse bias (HTRB) testing at 80% BV_{DSS} (breakdown drain-to-source voltage with source shorted to gate). Stressing at 175°C checks for possible changes in I_{DSS} and $V_{GS}(th)$. These tests are very sensitive in detecting possible mobile-ion contamination.

The reliability of the solder die-attach is monitored by power cycling devices between 30°C and 130°C while monitoring possible changes in thermal impedance.

Acknowledgments

The authors wish to express their appreciation to the many people, too numerous to mention individually, who provided support and made contributions toward the successful development of the power MOS-technology process and device family. These people are a part of the several research groups within Hewlett-Packard Laboratories (Integrated Circuits Lab, Integrated Circuits Processing Lab, Instrument Research Lab and Solid State Lab), and HP's New Jersey and Microwave Semiconductor Divisions.

Karl H. Tiefert

Karl Tiefert joined HP in 1972 with previous experience in working with high-power diodes and silicon-controlled rectifiers and beam-lead ICs. At HP he has done process and device development related to Schottky barrier, noise, and detector diodes and is now engineering manager for the power MOSFET production line. Karl has authored several papers and is a co-inventor for six patents related to semiconductor device technology. He is a native of Säckingen, Federal Republic of Germany and attended the Institute Juventus in Zurich, Switzerland where he earned the Engineering Diploma in electrical engineering in 1963. Karl is married, has one son and two daughters, and lives in a house that he and his wife built in Los Altos Hills, California. During his leisure time he enjoys soaring and jogging, climbing, and skiing with his family.

Robert L. Myers

Bob Myers joined HP in 1978 and developed GaAs FET amplifiers before his current responsibility as a senior applications engineer for power MOSFETs. His previous work experience includes microwave circuit design and work on a solid-state phased-array radar. Bob is a native of Amarillo, Texas and earned a BSEE degree in 1970 from Texas Tech University. He is married, has one daughter and one son, and lives in Cupertino, California. During his leisure time Bob is active in rifle and pistol target shooting and enjoys woodworking (he makes replicas of 17th and 18th century furniture).

Dah Wen Tsang

Dah Wen Tsang was awarded a PhD degree in quantum electronics by the University of California at Berkeley in 1978. He joined HP that same year and since then has worked on power MOSFET device design. Dah Wen is a member of the IEEE and Sigma Xi and has co-authored three papers about using Schottky diodes for infrared detectors and mixers. He is a native of Peking, China and lives in Union City, California. Dah Wen is married and has a newborn son.

Victor Li

Victor Li was born in Shanghai, China and attended Rice University in Houston, Texas where he earned the BA and MSEE degrees in 1972. He joined HP in 1973 and has worked in several areas related to the use of microwave semiconductor devices. Victor is an application engineer for the power MOSFET and has written several HP application notes. He is married, lives in Sunnyvale, California and enjoys playing tennis, photography, and music.

SPECIFICATIONS

HP Model HPWR-6501 Power MOSFET

ELECTRICAL SPECIFICATIONS (T_{case} = 25°C):

Symbol	Parameters and Test Conditions			Units
BV_{DSS}	Breakdown voltage (drain-to-source)	I_D = 0.1 mA, V_{GS} = 0	450	V minimum
I_{DSS}	Leakage current (drain-to-source)	V_{GS} = 0, V_{DS} = 400V	10	μA maximum
		V_{DS} = 360V	--	μA maximum
R_{DS}	On-state resistance (drain-to-source)	V_{GS} = 20V, T_C = 25°C, I_D = 3A	0.85	Ω, maximum
g_{fs}	Forward transconductance	V_{DS} = 20V, I_D = 3A	1.8	S typical
$V_{GS(th)}$	Gate threshold voltage	I_D = 1.0 mA, V_{GD} = 0	3	V minimum
			7	V maximum
I_{GSS}	Gate leakage current	V_{GS} = ±20V	0.1	μA maximum
C_{ISS}	Input capacitance	f = 1.0 MHz	1000	pF typical
C_{RSS}	Reverse transfer capacitance	V_{DS} = 50V	30	
C_{OSS}	Output capacitance	V_{GS} = 0	100	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200V, I_D = 3A	30	ns typical
t_r	Drain current rise times		20	
$t_{d(off)}$	Turn-off delay time		60	
t_f	Drain current fall time		15	
θ_{JC}	Thermal resistance, junction-to-case		1.39	°C/W maximum

MAXIMUM RATINGS:

Symbol	Parameter		Units
V_{DS}	Voltage, drain-to-source	450	V
I_D	Drain current, continuous	6	A
I_{DM}	Drain current, pulsed	12	A
V_{GS}	Voltage, gate-to-source	±40	V
P_D	Power dissipation	90	W
I_L	Drain current, clamped inductive	6	A
T_J (oper)	Junction operating temperature	-55 to +150	°C
T_{stg}	Storage temperature		

PACKAGE: Conforms to JEDEC outline TO-3.
PRICE IN U.S.A.: HPWR-6900 Designer's Kit (two HPWR-6501s, data sheet, capability brochure, and applications literature), $46.50.
MANUFACTURING DIVISION: MICROWAVE SEMICONDUCTOR DIVISION
350 West Trimble Road
San Jose, California 95131 U.S.A.

MOSFET Fabrication Requires Special Care

The high gate density and the large area of a vertical power MOSFET cause the fabrication yield to be sensitive to contamination and processing problems similar to those in MOS LSI manufacturing. The key problems that can prevent the production of high-quality products with adequate yields are:

1. Sodium contamination (Na^+)
2. Particle contamination
3. Process step irregularities, and
4. Photomasking defects.

To eliminate these problems requires manufacturing in an ultra-clean semiconductor facility (Fig. 1).

To avoid Na^+ contamination, all chemicals used during the manufacturing process have especially low Na^+ content and the process procedures are designed and executed to keep Na^+ contamination levels as low as possible. This is necessary because the gate threshold voltage $V_{GS}(th)$ is extremely sensitive to any sodium contamination that reaches the gate region. One grain of table salt (NaCl), for instance, contains enough sodium (if evenly distributed) to contaminate devices on more than 250,000 three-inch-diameter wafers to the point where $V_{GS}(th)$ shifts greater than 1.0V occur.

To assure long-term device reliability, especially the stability of the threshold voltage, the devices are passivated with a silicon nitride layer, an excellent barrier against Na^+ contamination.

To eliminate particle contamination all wafer handling is performed under clean, laminar air flow conditions. To maintain the necessary low particle density (less than 350 particles/m^3) all fabrication area personnel conform with a strict dress code that requires that hair, hands, clothing and shoes be covered with clean, particle-free protective clothing (Fig. 1).

To address the problems of process irregularities extensive use is made of computer-controlled equipment. A master computer with a series of terminals allows constant access to all process specifications. This system, called PCS (Process Control System), was developed by Hewlett-Packard Laboratories.[1] PCS is also used for tracking lots and providing yield and run history information. All high-temperature processes, such as diffusion and low-pressure chemical vapor deposition (LPCVD), are carried out in computer-controlled furnaces (Fig. 1c). This control covers not only temperature, gas flows, and push-and-pull rates, but also the proper sequence of individual process steps. Photomasking defects are minimized by the use of high-quality photoresist, solvents and masks in an especially low-particle-count environment. The photomasking is also done with a computer-controlled system that dispenses and spins on photoresist, softbakes, develops, rinses, and hardbakes wafers automatically. A projection mask aligner for alignment and exposure of the various layer patterns is an integral part of this system.

Reference

1. C. Clare, "A Process Control Network," Hewlett-Packard Journal, June 1981.

Fig. 1. *(a) Planar magnetron system used for metal deposition. (b) One of the wafer etching and cleaning benches. (c) Loading wafers into low-pressure chemical-vapor-deposition (LPCVD) system.*

Power Line Disturbances and Their Effect on Computer Design and Performance

Noise induced on the ac power line by machinery, lightning, and even appliances can be deterimental to computer performance. By becoming familiar with the nature of the noise and its causes, the designer and user can take steps to minimize the effect on computers.

by Arthur W. Duell and W. Vincent Roland

ONE OF THE EARLIEST and continuing problems with computer systems is ac power line disturbances on customer premises. The computer manufacturer is becoming increasingly concerned about the ac line transient and grounding environment that a computer system is subjected to at a customer site. Designing for immunity to power disturbances becomes prohibitively expensive if all of the conceivable power configurations and electrical noise sources are considered. For example, a forty-year-old house converted to office suites will probably not have third-wire grounding because that type of wiring was not required when the house was built. This particular situation is a problem because adequate grounding within and for a computer system is an integral part of the system design and must be considered for any computer installation.

If ac power line disturbances are not considered in the basic design or as part of the customer installation, the effects of a power anomaly may appear in many forms. The equipment may cease to operate, errors may occur in normal processing cycles or be introduced into data files and programs, or hardware damage may occur. A 10-millisecond power failure affects a period of time during which 10,000 computer operations may be performed.

The resolution of problems caused by ac power disturbances requires characterization of the ac power source and determination of the computer system's sensitivity to such anomalies. The effect of any possible solution on the manufacturer and the customer must be evaluated. If the manufacturer incorporates devices to protect the computer against all of the possible ac disturbances the initial cost of the computer increases significantly. A dilemma arises if, to keep purchase costs low, this is not done. In the purchase of any computer system, the cost of ownership must also be considered. The customer wants and should expect maximum use with a minimum of maintenance and downtime. If the computer is unable to handle power anomalies, the downtime and maintenance can become excessive and the cost of ownership increases dramatically.

Therefore, some compromise is required to minimize the overall cost to the customer. The customer should help by improving the environment for the computer system installation. The manufacturer should correctly and economically specify the environment required and educate the customer about this specification in addition to incorporating economical design features that improve the computer system's resistance to ac power line disturbances.

Characterization of Power Sources

Improving the immunity of a computer system to electrical noise requires adequate characterization of the ac power source. The terms frequently used to describe power line anomalies are discussed in the box on page 27. The noise

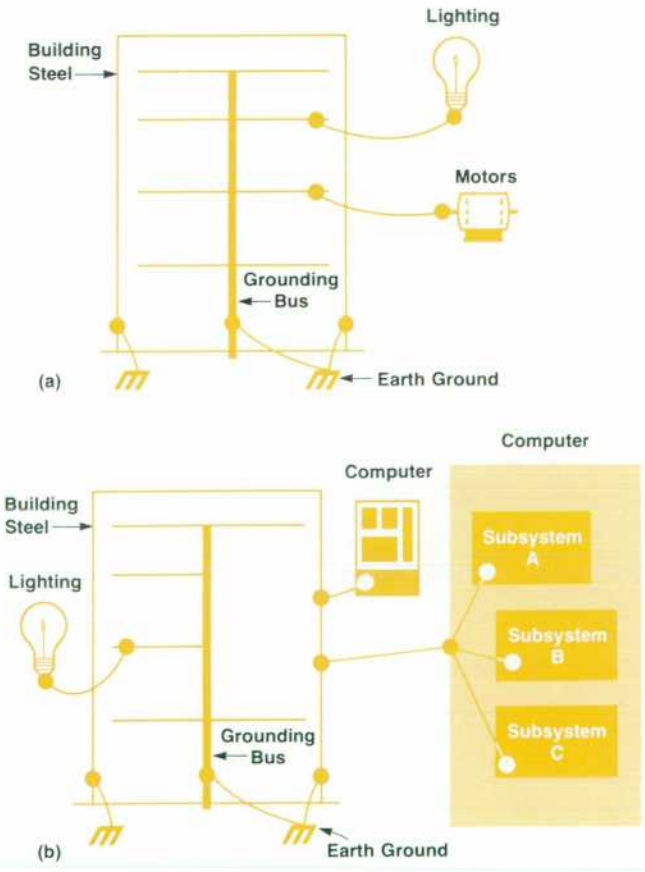


Fig. 1. *The grounding within a building can consist of both (a) single-point (used for lighting, motors, and appliances) and (b) multipoint (used for computer systems) ground bus systems.*

present on an ac line can be generated by conditions unique to the customer's environment and by variations typically found on any power line supplied by a public utility. Wiring codes developed by regulatory agencies to insure the safety of the user are often in conflict with line configurations designed for noise reduction.

Computer manufacturers and users cannot influence or change these facts significantly. To place these conditions in proper perspective, computer systems and other sensitive control loads represent less than 0.01% of the total utility load. Consequently, it is understandable that a utility will not try to prevent power disturbances affecting computers. Wiring codes are also generated with respect to the general consumer. Generally wire sizes and grounding specifications are based on electrical loads associated with major appliances and heavy electrical machinery, and do not take into consideration the low impedances that are required when computer systems are switching at millisecond speeds.

Factors describing the quality of an ac power line are nominal line voltage, service voltage, utilization voltage, statistical distribution of transients generated by the utility and the customers, and regulatory body specifications. In the U.S.A. there are national standards developed by American National Standards Institute (ANSI), and these specifications are typically used by U.S. utilities to permit better networking and interchange of power.

Nominal line voltage is the level close to the average value expected during normal operation. This value, measured at the outlet, varies with geographic location.

The most important parameter that the utility must adhere to is the service voltage—the voltage supplied to the customer's meter. In the San Francisco Bay area it is 114 volts minimum to 126 volts maximum. For three-phase-wye distribution, it is 197 volts minimum to 218 volts maximum. Generally speaking, the three-phase line voltage will be lower than the nominal 208 volts, but the power company is still within specifications as long as the line voltage does not go below the minimum service voltage.

The utilization voltage (at the wall outlet) is 110 volts minimum to 125 volts maximum. For three-phase-wye distribution, it is 191 volts minimum to 216 volts maximum. Herein lies a difficulty. The building owner is responsible for all internal wiring within the building from the meter to the wall outlet. Therefore, if there is a problem with the voltage, it is of little value to a user to have the power company measure voltage at the wall outlet because they have no control over the internal wiring of a building.

To compound the problem, there are some studies being made by U.S. utilities to change generating voltages to conserve energy. The federal government is strongly suggesting to the utilities that there be a conservation voltage reduction. This is a systematic lowering of distribution voltages to reduce energy consumption by customers. The minimum service voltage would remain the same but the maximum would be lowered. Suggested ranges would be either 114 to 118 volts or 114 to 120 volts. When the generating margin narrows, the utilities are forced to do more load switching. The result is more transients.

It is impossible to quantize transients caused by utilities switching loads during peak demand hours, or by breaker action during some fault condition. A model can be developed, but it is a function of such parameters as line impedance, circuit breaker size, fault current, and other widely varying factors. Obviously, the computer installer and customer should be fully aware of possible problems when the computer system is installed near a utility substation or switchyard.

Customer Site Characteristics

Noise on the power line can be generated in many different ways at the computer user's site. Electric clock systems signal-modulate the power distribution within a facility once an hour to update all electric clocks. Flicker (momentary voltage dip due to the starting of a large appliance) can occur typically 10 times per hour and the duration can be from 160 to 670 ms. The maximum amplitude of a transient is directly proportional to the velocity with which a contact opens, and is independent of power consumption. A 400-hp motor (with large slow-moving contacts) produces transients with one-tenth the amplitude of those produced by an electric clock motor. Fluorescent light switching can cause an extended transient of 2-MHz, 500V oscillations lasting for 20 μs. Power characteristics of an installation change with time even though good site preparation is done initially. Vending or copy machines can be added inadvertently to circuits and grounding that were initially wired exclusively for computer systems.

The most common customer problems associated with ac power are nonisolated grounds and improper conductor sizes. These occur even when the grounding and wiring are done according to code.

Two categories of ground systems must be considered:

1. Safety (dc conduction)—the electrical power grounding system which includes all ac power, distribution and utility service power used for lighting, equipment power, et cetera.
2. EMI (RF conduction)—signal circuit grounding which includes all electronic and electrical control circuits

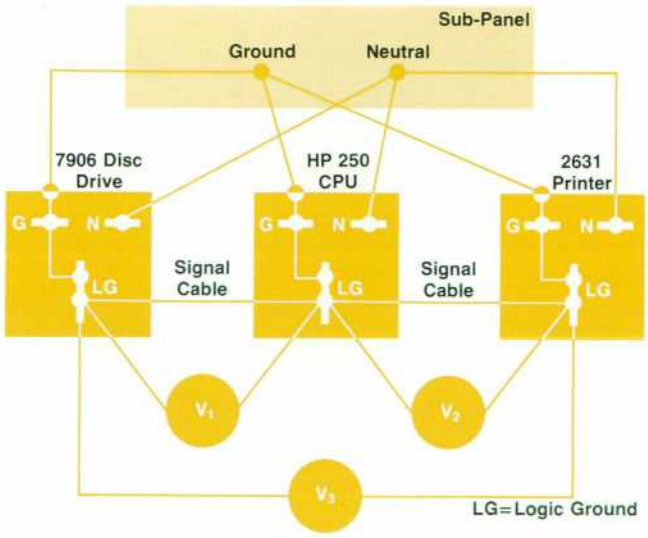


Fig. 2. *Voltage differences between the logic grounds of interconnected computer units can exist if ground impedances and power needs differ between any two units.*

Definitions: ac Power Anomalies

Power line disturbances may be classified into several types (see Fig. 1):

Voltage variation: The supplied voltage deviates from the prescribed input range. Input below the range is a sag, above is a surge. Sags can be caused by deliberate utility cutbacks (brownouts) to lower power consumption, by customer loads for which the utility cannot compensate, or by an excessive inrush starting current to powered-up equipment. Surges originate from utility line malfunctions or sudden changes in power demand (removal of heavy loads) which cannot be corrected instantaneously.

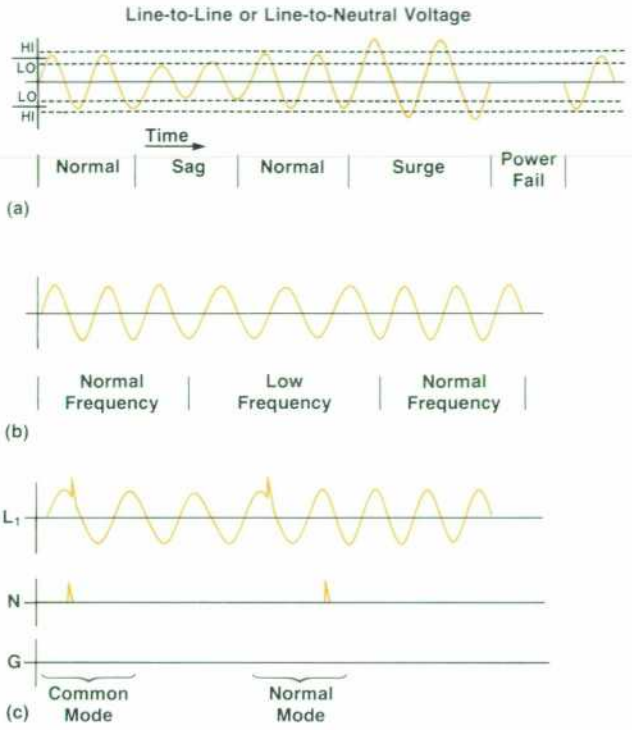


Fig. 1. *Graph of the ac line voltage under (a) normal, sag, surge, and powerfail conditions, (b) normal and abnormal frequency conditions, and (c) with common-mode and normal-mode transients.*

Frequency variation: The frequency of the power line voltage deviates from the prescribed input range. Sudden changes in load to the utility, switching of power between utility companies, or generator malfunction can cause such variations.

Powerfail: Total removal of the input voltage to the computer for at least 5 ms. Switching of power by utilities, either for the purpose of redistributing loads or correcting short circuits, will produce power failures from a few cycles to several seconds. Power equipment failure can result in outages of minutes to hours.

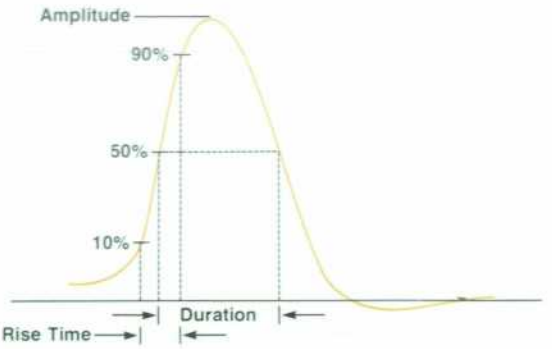


Fig. 2. *Characteristics of transient noise on an ac power line.*

Transient: A disturbance of less than 5 ms duration. The amplitude, rise time, duration, resultant oscillation (if any) and repetition rate (see Fig. 2) determine the effect on the computer's operation. We can classify transients into three types, distinguishing them by their sources.

Transients from nearby sources (within 50 feet of the computer) have very fast rise times (nanoseconds) rich in high-frequency content. The power cord becomes a transmission line, and the propagation of the transient is influenced by distance, conduit, adjacent conductors (into which these transients may be coupled), flatness of the cord against the floor, and socket connections. Because of high-frequency coupling between the conductors in the cord, these transients are usually common-mode by the time they reach the computer. Sources of this type of transient are anything with mechanical breaker contacts, such as coffee pots, electric typewriters, and clock motors.

Transients produced by distant sources will have slower rise times (microseconds) and longer durations than the first type. They are generated by any electrical device that produces enough transient energy to propagate through the device's circuit breaker and distribution panel back to the circuit breaker feeding the computer. Elevator motors, industrial machinery (either on the premises or a block away), and air conditioners are possible sources. These transients are normal-mode or common-mode.

Other transients with rise times similar to those of distant-source transients and with a common-mode structure can be produced by utility distribution faults and resultant arcing, or by lightning, direct or induced, on the utility power pole.

associated with a computer system.

In the first category, all neutral and ground line distributions are wired on separate buses and connected together at the main power transformer entrance to the building, making a single-point ground.[1] In the second category, the ground from the electronic equipment is connected to the nearest steel structural beam to make a multipoint ground (see Fig. 1) from a facility viewpoint.

Because computer systems typically use earth ground as a reference within each cabinet and the entire system is connected to the facility earth ground, it is very important that the computer system be connected to an EMI grounding system. Fig. 2 shows the system power and interface cable hookups and points where common-mode noise (voltage between both lines and ground) can exist. The net voltage difference between any two points on the ground network usually will be small (1 to 3 volts). However, the current through certain network paths can be on the order of 3 to 5 amperes with occasional currents of 10 to 15 amperes.

For typical building wiring, electricians use water pipes

and conduit as ground. For safety and minimal shock hazard, this is legal from an electrical code viewpoint. For EMI suppression it is inadequate because lighting loads, vending machines, and other types of office equipment are connected to the same grounding system. Another common contributor to stray ground currents within a facility is the connection of the ac neutral line to earth ground inside the branch panel. Then the ground network becomes a part of the ac return line to the main building service entrance. The line current will divide between the neutral line and the ground return network in inverse proportion to the impedance of the two paths.

Because instantaneous power surges are required by a computer system during turn-on and normal operation, wire sizes must be large enough to keep the voltage from sagging. For example, during computer turn-on, switching power supplies can require currents peaking at 150A and decaying exponentially to 20A in less than 30 ms. If the wire size is inadequate, the input voltage can sag below the required input voltage tolerance of the computer for a period of 100 ms, causing the power-control circuitry to detect a powerfail, thus shutting the system off. Wire sizes specified by typical code requirements are usually at least one size smaller than required for computers. Such code requirements make it difficult for the computer manufacturer to convince the customer and electrician that larger wire sizes must be used if the computer system is to operate satisfactorily.

Computer System Sensitivity

Circuits used in a modern computer system are extremely fast and more vulnerable to noise than circuits used a few years ago. Because there is the same high-frequency sensitivity in a peripheral as in the mainframe, the same design parameters are used to immunize the total system from outside disturbances. For software, data integrity is protected from power line transients by using various error correction codes (ECC) in the transmittal of data between parts of a system, and "disc retrys" are used on disc drives when errors occur. Therefore, power line noise can be masked by using software error-correction techniques.

To achieve less susceptibility to power line noise, larger systems (costing more than $200,000) often use motor-generator sets for the power sources. These sets are purchased as part of the system, and can provide a near-perfect power source. Small computers containing the same type of internal circuitry are subjected to the same types of power disturbances as the larger computer systems, but instead use ac input filter design or components such as metal-oxide-varistors (MOV) to improve noise immunity.

Impact on Customer and Manufacturer

Making positive determination that a computer installation problem is caused by power line disturbances can be very difficult. The occurrence may be random, and the effects on the system may be different depending on the state of the electronics at the precise time of the disturbance. Symptoms of such problems overlap with those that may be caused by intermittent electrical connections, electrostatic discharge (ESD) either directly to the computer or indirectly via other objects in the immediate vicinity, or even software program bugs. If intermittent ac disturbances are suspected, isolating them may require expensive monitoring equipment that is installed for a period long enough to detect the next occurrence.

The time required to analyze and repair an ac line disturbance problem can be several times the hours required for analysis and repair of other service problems. During the process of diagnosis machine time is lost and the service engineer may have to visit a site several times before proper remedies can be made. In the case of ac power transients, which can be random and are unpredictable, direct correlation of cause and effect is extremely difficult to obtain.

Detection of a Noise Problem On-Site

The service engineer's objective is to prevent power line disturbances from reaching the computer by discerning their characteristics, and then either remove the source or isolate the computer from the source. A comprehensive set of site preparation guidelines is sent to the customer prior to delivery of a computer system. If the guidelines are followed, the likelihood of power line disturbance problems is minimized. The service engineer may participate in site preparation with the customer. Whether during a site preparation or installation, or in troubleshooting an installed system, a service engineer may proceed through the following steps:

- Look outside the customer's site. Check for major industries in the area that consume large amounts of electricity. Their operation can cause voltage variations or transients to be propagated to other users sharing the same output of the utility company's substation transformer.
- Look within the customer's site for heavy electrical equipment. A transient source within the site may affect

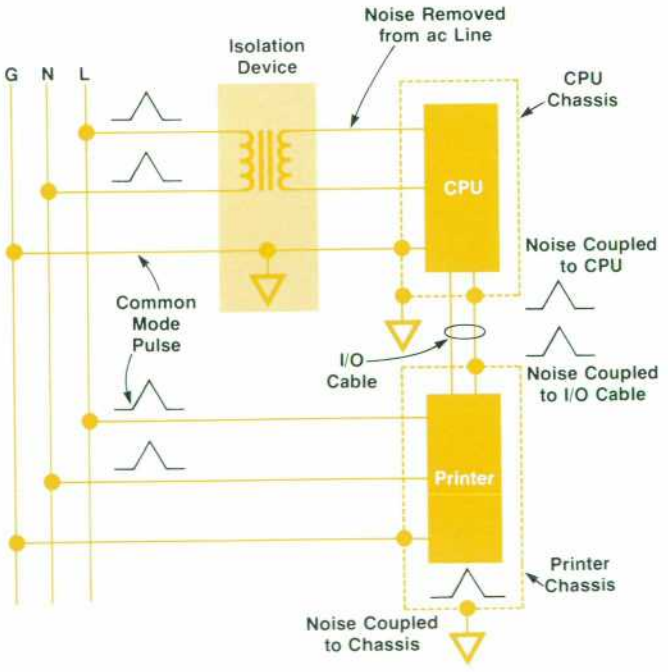


Fig. 3. *All units in a computer system must be isolated from the ac power line. Otherwise, an unisolated unit, the printer shown here, can couple noise to an isolated unit, the CPU here, via the I/O interconnections.*

the computer installation more severely than a distant source because nearby transients, especially fast-rise-time pulses, do not dissipate significantly in the short distance before they reach the computer.

- Note local weather conditions. Electrical storms may cause transients by direct lightning hits on utility lines or induced coupling through nearby earth strikes. Besides the transients, the utility company's hardware is sometimes affected, causing voltage variations or powerfails.
- Check the wiring from the building's utility power connection to the outlets in the computer room. Feedback from HP's systems specialists in the field indicates that improper site wiring is often the major cause of power line disturbance problems. With the help of an electrician who is aware of local codes, check the building's electrical layout, and look for load distributions that overload any circuits, or branch circuits that allow other electrical devices to use the same circuit breaker as the computer. Distribution and breaker panels must have solid electrical connections, and breakers and wire capacities must equal or exceed the computer's demand.
- Check equipment layout at the computer installation. All devices must be plugged into their own wall outlets. Extension cords with multiple outlet boxes must not be used. If possible, avoid extension cords altogether. Check especially for grounding of all devices by having the electrician confirm that the ground wire is continuous back to the building's service entrance. A computer system can pollute its own power if these procedures are not observed.

Up to this point all checks have been visual. If no answers are obvious, measurement equipment is required. Tools for analyzing ac power become progressively more complicated and expensive as the problem becomes more difficult. First, wall outlets can be checked for proper polarity of the lines and ground, and for existence of ground by a receptacle-circuit tester. At the same time, a ground loop impedance tester (GLIT) can be used to test the integrity between the neutral line and ground. However, it only checks impedance at the line frequency, not at high frequency or RF.

When intermittents occur, the cost of the tool goes up significantly and requires the user to have some skill and training in its operation. Such a tool is a power line monitor

Table I
Features of ac Line Protection Devices

Device	Description	Voltage Variation Protection	Frequency Variation Protection	Powerfail Protection	Normal-Mode Transient Protection	Common-Mode Transient Protection
Shielded isolation transformer	A transformer with isolated, electrostatically shielded primary and secondary windings.	Input/output ratio can be manually selected by jumpering windings.	None	None	Low. Transformer windings may limit bandwidth, but pulses get through.	High. 120 dB CMR specifications are available.
Tap-switching line conditioner	A shielded isolation transformer regulating output voltage by automatically switching additional secondary windings in or out.	Good. For a broad input range (≈40% tolerance), the output is kept within a ≈15% range.	None	None	Low to medium. Additional filtering may be provided by filter capacitors.	High. 120 dB CMR specifications are available.
Ferroresonant line conditioner	A shielded isolation transformer using a saturated core to clamp voltage to a set-level, and reconstructing the ac sine wave in the secondary.	Good. For a broad input range (≈30% tolerance) the output is kept within a ≈2% range.	None, and will itself malfunction if frequency varies by more than a few Hz.	Low. Energy storage in the core may help if the duration is less than one cycle.	High. Saturated core clamps all pulses. 120 dB NMR specifications are available.	High. 120 dB CMR specifications are available.
Uninterruptible power source (UPS)	Either a motor-generator set, with a diesel engine backup, or a solid-state inverter powered by dc from storage batteries.	High. Alternate power source cuts in if ac line is insufficient.	High. Alternate power source cuts in if ac line is insufficient.	Very good. Duration protection is a function of engine fuel reserve or battery capacity.	Total isolation.	Total isolation.

which can be left at a customer site for several days and will measure and record voltage surges, sags, frequency variation, powerfails, and transients. Measurements are logged on a printout with their times of occurrence.

Throughout the measurement process, the service engineer notes the nature of the disturbance and checks it against factory-supplied specifications for the computer.

After these checks are completed, a solution is likely to be evident. It may be one of two types: 1) the problem source is identified and can be removed, or 2) the source cannot be removed or cannot be identified, but the nature of the disturbance has been characterized and a device to isolate the computer can be specified.

Isolation Devices

Isolation devices are available with a variety of features to match the needs of the problem site. Manufacturers offer product lines with varying degrees of protection and power handling capabilities. A qualitative summary of features is given in Table II.

Isolation devices must be installed with full knowledge of their capabilities in mind. Large computer sites set up through subcontractors place no burden of installation (other than financial) on the customer. Customers doing their own installation, however, must work with the service engineer to fulfill the prerequisites before successful operation can happen. Isolation transformers and line conditioners, in particular, are not panaceas that are merely uncrated and connected between the computer and the wall outlet. These devices have their own input and output specifications that must be met, or else a new set of problems will emerge to replace the old ones. All devices in the computer system should be isolated. Otherwise, as shown in Fig. 3, an unprotected system component can receive a transient on its ac input and couple the noise to its chassis. Then the noise is coupled to an I/O cable leading to the chassis of the "protected" component.

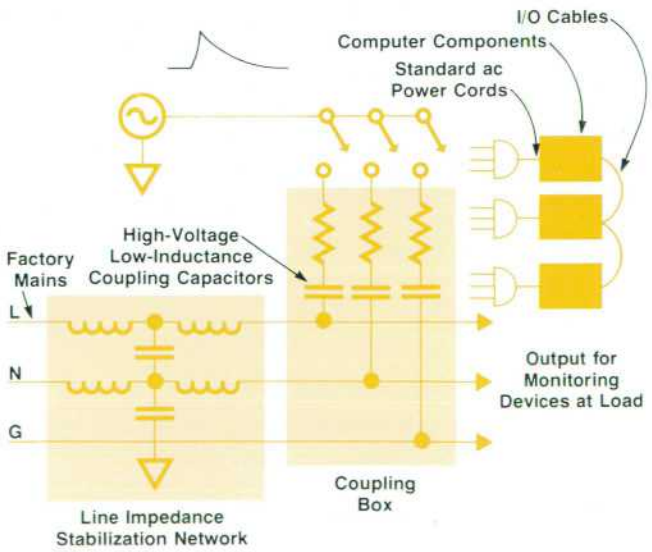


Fig. 4. *Equipment sensitivity to transients can be evaluated by injecting pulses onto the power lines using the simplified test arrangement shown above.*

Factory Action to Minimize Susceptibility

The key factor in effective factory design and testing for ac disturbance immunity is realistic simulation. Underdesign will result in dissatisfied customers and high warranty costs, while overdesign may inflate the manufacturing cost (and thus selling price) with no perceived increase in performance. Objective data on the nature of disturbances is scarce. HP's test procedures have been developed based upon published data[2-6] and feedback from service engineers. Test specifications at HP's Business Computer Group fall into four categories:

- Input voltage test. Using a variable transformer, the device is tested over a prescribed tolerance about a prescribed design center, or nominal value. Most of the computers have nominal input values of 100, 120, 220, and 240 volts ac rms. The tolerance about each of these values is +5%, −10%.
- Input frequency test. A solid-state power amplifier whose output tracks the frequency of a variable oscillator supplies power to the tested device. Computer equipment electronics generally has little difficulty in meeting a specification of 47.5 to 66 Hz. Devices with ac synchronous motors, or terminals with a fixed CRT sweep rate, will experience problems if the frequency varies more than 1 Hz from the design center.
- Powerfail test. The computer is tested for reactions to momentary removals of power. For test repeatability, semiconductor devices in series with the ac line are used to interrupt the power under control of an electronic timing generator. Durations of less than one cycle (20 ms) should have no effect on operation of the product. Greater durations may initiate an automatic shutdown procedure. An absolute rule is that no data be lost. In the case of computer semiconductor memory, batteries provide backup power for at least 15 minutes. Flying-head disc units retract their heads before shutting down.

  Real-world powerfails can be of any duration, and the power supply hardware must be able to respond properly to restoration of power at any time during its power-down sequence. Otherwise, the supplies and their control logic may hang in a shutdown state, requiring a second removal of power (for a longer duration) to clear the condition. Further, a powerfail event may occur in the midst of a low-line-voltage condition near the bottom of the specified operating range. This combination must not affect recovery performance.
- Line transient tests—Pulse generators are used to inject energy into the ac line input. A test arrangement is shown in Fig. 4. More than for any other power disturbance test, the choice of specifications for this test is difficult to substantiate. Although the numeric parameters used by HP are proprietary, the general test procedure is:
  1. Apply the following types of transients: high-speed common-mode, slow-rise-time normal-mode, and slow-rise-time common-mode.
  2. Apply pulses of positive and negative polarity, and vary pulse timing relative to the phase of the ac wave.
  3. Gradually increase amplitude of the applied pulse until a failure occurs, or the test specification limit is met.
  4. During the test, the system runs programs that exten-

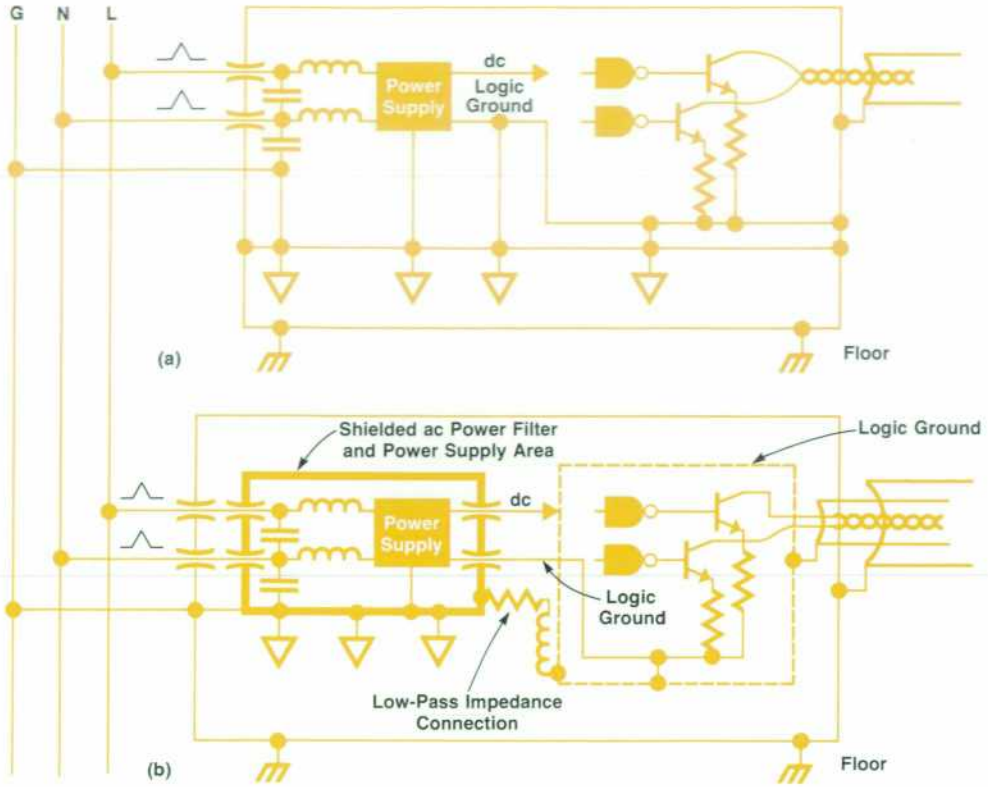


Fig. 5. *Two grounding approaches can be used to increase immunity to line transients. (a) Common safety and logic grounds. Transient energy is uniformly distributed throughout the chassis so that no noise potentials exist between the internal circuits. (b) Isolated safety and logic grounds. Transient energy is tightly coupled to the chassis, but the internal circuits are isolated with respect to the chassis by a low-pass filter.*

sively exercise the hardware and report errors the moment they occur.

A similar procedure is used in the evaluation of isolation devices or shielded ac power cords and I/O cables. In all cases of factory testing, once the operating limit of the system is found, measurements are logged for reference in case consultation with the field is necessary.

Future Trends

Computer manufacturers must prepare themselves for two evolving challenges from ac power line disturbances. First, commercial power from the utility companies is going to become less stable and reliable than at present. This is not by design of the utilities, but a consequence of rising customer demand that outpaces the growth of the utilities' capability. As the unused power margin of the utilities dwindles, rotating blackouts and brownouts may be used, and power will be borrowed from other regions. Second, the shrinking prices of computer technology will bring it within the realm of users who cannot afford, and do not care to understand, electrical site preparation for their computers. The tendency of designers to achieve lower cost by lowering ac power performance expectations and associated hardware costs must be resisted. In fact, an increasing percentage of new project investment must be addressed to this issue. Future computer system designs must also consider the increasing susceptibility of internal components to transients because of their higher operating frequencies. The use of undedicated wall outlet power, which implies sharing power with other office appliances, must be considered because of the increasing portability of computers and peripherals.

One approach to achieving transient immunity requires meticulous care in the design of front-end filters for each component in the system. If the filters are to be effective, the grounding and ground reference within a cabinet must be free of electrical noise so that the filters will have a low-impedance plane for discharging unwanted transients. Fundamental to the design of computer systems is the elimination of ground loops between peripherals and the computer. The present use of single-point grounding (isolated ground) for the total system is a brute force method. Product designers can choose from two alternative grounding approaches to maximize immunity to line transients. The first approach bonds chassis and logic grounds together at many physical points. Any transient signals entering the system are thus coupled to both grounds simultaneously. The product's entire contents momentarily rise in potential relative to its surroundings (see Fig. 5a), although within the product no noise potentials will exist. When such products are connected via I/O cables, problems may result. Unequal coupling of transient energy to the cabinets can create a potential across the logic grounds of the cable transceivers which may cause incorrect data transmission.

The second approach requires total separation of the cabinet safety ground and logic ground except for one connection through a low-pass filter (Fig. 5b). All incoming transients are coupled to the chassis frame by the input filters as before, but they do not couple to logic ground (except by radiation). Circuits therefore remain quiet with respect to other devices that may be connected by cables, although the chassis frame may momentarily have a potential. Double-shielded cables may be necessary, with the outer shield connected to each chassis and the inner shield

connected to logic ground. This technique requires that all devices in the system follow the same scheme.

Other system design techniques are:

- High-frequency power distribution to I/O devices. Hewlett-Packard has implemented this design in the HP 1000 L-Series Computers. A 25-kHz single-phase power distribution system is transmitted to various remote components of the total computer system. The high-frequency ac power is converted to dc power at the remote device to reduce ground noise coupling between the central processing unit (CPU) and sensitive I/O devices.
- Optical isolators at each end of a wire cable to reduce or eliminate common-mode noise between system components. Thus, the signal returns are returned to the source of the signal instead of being connected with the ground at the receiving end. Optical interfaces can pass dc as well as pulse-type signals (this technique is used to connect terminals to the HP 250 computers). Fiber optic cables can be used instead of wires to form a wholly optical interface between system components.

Acknowledgments

We would like to express our thanks to Jim Gillette at the Data Systems Division, whose detailed research and summarizing of various papers, including the references listed below, originated new thoughts on test and specification procedures. Larry Rea, formerly of the Customer Engineer Organization, provided valuable inputs based upon experience with solving customer problems, and Jim Brannan in our reliability group has been instrumental in building the customized system-level test tools. Norm Marschke, Computer Systems Division, has made significant contributions in design of system noise immunity and power-control circuits for new HP products.

References

1. H. Denny and J. Moody, "Considerations in the Design of a Grounding System for a Complex Electronic Facility," IEEE Electromagnetic Compatibility Symposium Record, July 1974, pp. 85-91.
2. J. Hull and W. Wethercot, "The Frequency of Occurrence and the Magnitude of Short Duration Transients in Low-Voltage Supply Mains," The Radio and Electronic Engineer, September 1964, pp. 185-190.
3. W. Hayter, "High Voltage Nanosecond Duration Power Line Transients," San Jose Testing Laboratory, International Business Machine Corp, Technical Report S-1117, November 13, 1964.
4. F. Martzloff and G. Hann, "Surge Voltages in Residential and Industrial Power Circuits," IEEE Transactions on Power Apparatus and Systems, July/August 1970, pp. 1049-1056.
5. "World Electricity Supplies," British Standards Institute, 1974. (Through Technical Export News, a service of the British Standards Institute.)
6. G. Allen and D. Segall, "Monitoring of Computer Installations for Power Line Disturbances," IBM Corporation, 1973 IEEE Power Engineering Society winter meeting, New York, New York, January 1974, Paper C 74 119-6.

W. Vincent Roland

Vince Roland, a native of Louisville, Kentucky, is a graduate of the University of Louisville, where he received the Master's degree in electrical engineering in 1973. He then joined HP and has worked in several of HP's divisions. Vince is now the product assurance hardware engineering manager at HP's Computer Systems Division. He is a member of the IEEE, married, and a resident of Sunnyvale, California. Vince is an active church member and enjoys photography, which he does as a spare-time business.

Arthur W. Duell

Art Duell came to HP in 1972, did technical writing and support for the HP 2000 Computer, was a service engineer for the HP 300 Computer, and now is a service engineer for the HP 250 Computer. His previous work experience was in circuit and system design. Art earned the BSEE degree in 1957 from the University of Colorado and has done graduate work at the University of Santa Clara, California. He is a member of the IEEE and co-hosts HP's computer systems group on ac power. A native of Windsor, Colorado, he is married and has two sons. Art is an active church member and enjoys skiing and fishing. He and his wife are busy remodeling their 30-year-old home in Cupertino, California.

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

Bulk Rate
U.S. Postage
Paid
Hewlett-Packard
Company

HEWLETT-PACKARD JOURNAL

AUGUST 1981 Volume 32 • Number 8

Technical Information from the Laboratories of Hewlett-Packard Company

Hewlett-Packard Company, 1501 Page Mill Road
Palo Alto, California 94304 U.S.A.
Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
1181 KK Amstelveen, The Netherlands
Yokogawa-Hewlett-Packard Ltd., Suginami-Ku
Tokyo 168 Japan

CHANGE OF ADDRESS: To change your address or delete your name from our mailing list please send us your old address label. Send changes to Hewlett-Packard Journal, 1501 Page Mill Road, Palo Alto, California 94304 U.S.A. Allow 60 days.