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In this Issue:

A network analyzer for the R&D lab, a rugged, sealed terminal for the shop floor, a family of printers for the automated office. These products may not seem to have much in common, and they don't, except that they're all made by Hewlett-Packard and you can read about them in this issue.

The HP 3577A Network Analyzer measures the transmission and reflection characteristics of electronic components and networks over a frequency range of 5 hertz to 200 megahertz and displays the results on its built-in CRT, as shown in the cover photo. This high-performance instrument is being used by designers and manufacturers to test telecommunications equipment, mobile radios, video equipment, audio equipment, medical instrumentation, power supplies, disc drives, modems, amplifiers, attenuators, cables, crystals, integrated circuits, transducers, transformers, and many other devices. The HP 3577A story is a story of skillful, state-of-the-art design. Its bandwidth, dynamic range, accuracy, resolution, and sensitivity are as good as you'll find in this kind of product. It makes complex measurements easy to set up and perform. It manipulates results to its user's liking without a computer, but it can also operate under computer control. There's no magic behind any of this, just good design. Precise analog design for broad bandwidth. Digital signal processing for accuracy and display flexibility. Microprocessor control for simplicity of operation. For the details, read the articles on pages 4, 17, and 21.

The HP 3081A Industrial Workstation Terminal, described by its designers in the article on page 25, is a compact, personal miniterminal designed for low-cost factory data collection. It has big keys that are easy to operate with gloves on, and it's protected against dust, dirt, grease, oil, and liquids. You can clean it with any liquid soap or detergent and rinse it off with a hose, if you want to. This is where the automated factory begins—with data collected at the source, on the shop floor. An optional bar code wand, also sealed, lets the terminal read two types of bar code, increasingly recognized as the best way to speed the flow of parts and paperwork in industrial applications.

The new printer family consists of the HP 2932A General-Purpose Printer, the HP 2933A Factory Data Printer, and the HP 2934A Office Printer. They're all dot-matrix impact printers, capable of printing on multipart forms. All of the printers can print text at 200 characters per second and graphics with a resolution of 90 dots per inch. The HP 2933A can also print bar code and large characters (up to 28 times normal size), while the HP 2934A offers all these features plus near letter-quality printing and a wider choice of fonts. Letter-quality printing is done at 67 or 40 characters per second using a 36-by-24-dot character cell instead of the standard 9-by-12-dot cell. All three printers provide last-form tearoff, a paper-saving feature. In the articles on pages 30 and 33, the designers describe the three printers and the special integrated circuit that was designed for them. The integrated circuit makes sure that each printhead wire strikes the paper at the right times as the printhead sweeps back and forth across the paper, printing in both directions.

-R. P. Dolan

What's Ahead

Next month's issue, the last of 1984, will contain the annual index and four articles describing the design of the HP 3561A Dynamic Signal Analyzer. This versatile instrument allows the real-time study of geophysical, mechanical, acoustic, and electrical waveforms in the frequency range from 125 μHz (roughly one cycle every two hours) to 100 kHz. Its capabilities are, in a large part, made possible by custom-designed digital filter ICs.

An Advanced 5-Hz-to-200-MHz Network Analyzer

This instrument is a complete network analysis system containing an integrated three-input receiver subsystem, a graphics display, and a synthesized signal source. Softkey menus and a powerful operating system make it easy to set up and use.

by Robert A. Witte and Jerry W. Daniels

NETWORK ANALYSIS TECHNIQUES and instrumentation have advanced significantly from the early days of a room full of equipment requiring complicated adjustment and calibration for each measurement point. As circuits became more and more complex, the need for network analysis of greater accuracy and covering greater frequency ranges became more important. Fortunately, the increasing complexity and performance of the new circuits could, in turn, be used to simplify and improve the network analysis equipment used to design them. This synergetic process has resulted in the HP 3577A Network Analyzer and HP 35677A/B S-Parameter Test Set (Fig. 1), which bring a new level of performance/price ratio to network analyzer applications in the audio, video, baseband, IF, and RF frequency bands.

Features

The HP 3577A can be used either in stand-alone applications or as part of a larger instrumentation system. Its features include:

- A built-in source. This fully synthesized source has a frequency range of 5 Hz to 200 MHz, a frequency resolution of 0.001 Hz, and an output level adjustable from 15 dBm to −49 dBm.
- Three receivers (**A**, **B**, and **R**). Each receiver has a dynamic range of 100 dB and dynamic amplitude and phase accuracies of ±0.02 dB and ±0.2 degree for input levels of −10 dB to −50 dB relative to the maximum allowable input level.
- An annotated dual-trace display. Other display features include an autoscale function, markers, a choice of rect-

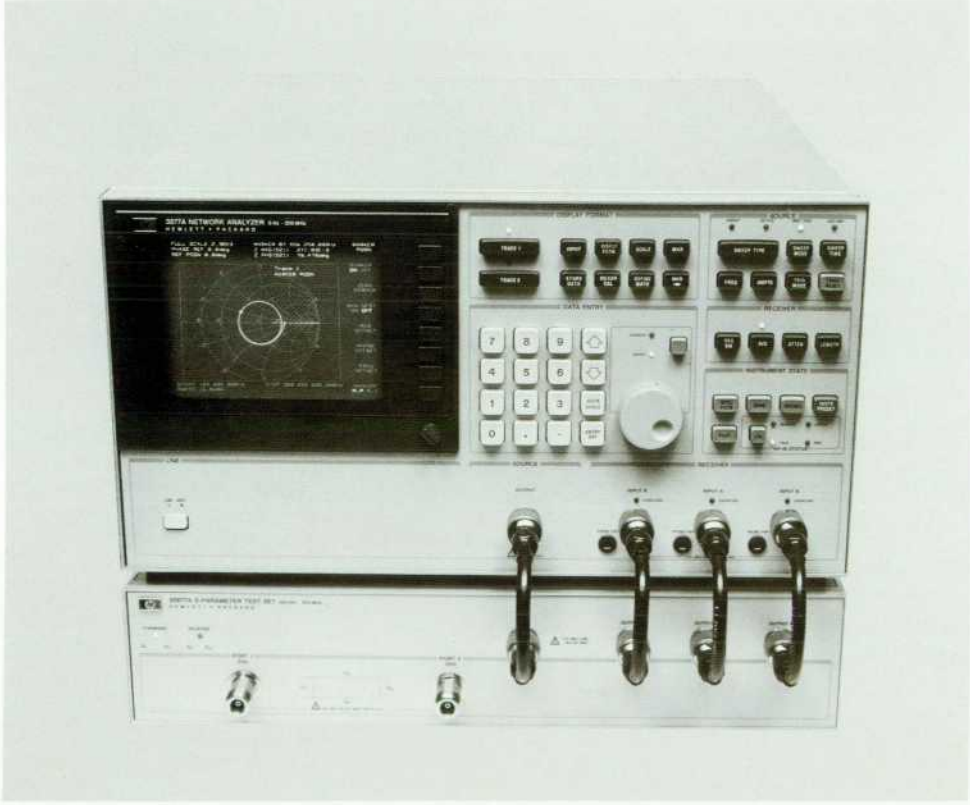

Fig. 1. *The HP 3577A Network Analyzer (top) provides cost-effective, high-performance network measurements. The companion HP 35677A/B S-Parameter Test Set (underneath) and a full line of accessories ensure a comprehensive measurement solution. Convenient softkey selection of measurement functions allows the user to measure transfer functions, magnitude/phase, insertion loss/gain, attenuation, electrical length, group delay, and gain compression.*

angular, polar, or Smith chart formats, and programmable graphics.

- Vector math operations. The HP 3577A can add, subtract, multiply, or divide user-defined combinations of input data, stored data, and user-defined constants and functions. The results can then be displayed without the need of a computer. (See box on page 8.)
- Full HP-IB (IEEE 488) programmability.
- Fast data transfer. Data can be sent rapidly to other systems in either ASCII or binary modes.
- Hard-copy output. Displayed data can be output directly to an external HP-IB plotter without need of a computer.

With the addition of the HP 35677A/B S-Parameter Test Sets (see article on page 17), comprehensive two-port device characterizations are possible.

Friendly Front Panel

The front panel is divided into five sections (refer to Fig. 1). The Display Format section determines how the data is presented to the user. This includes receiver input selection, scaling, the digital marker function, storage and retrieval of data, user-defined vector math, and measurement calibration. The Source section controls the frequency, amplitude, and sweep characteristics of the analyzer's output. The Receiver section sets up the receiver bandwidth, vector averaging, input attenuator, input impedance, and electrical length compensation. The Instrument State section is used to save and recall instrument states, dump data to a plotter, and exercise other assorted features. The Data Entry area is used to enter or modify all of the user-settable parameters in the instrument. Virtually all parameters can be entered using the ten-digit keypad, incremented up or down, or adjusted with the continuous entry knob. The knob can also be locked to the marker for convenience in positioning the marker on the display.

Because of the extensive feature set of the HP 3577A, its front-panel design is based on a softkey menu approach. Without softkeys, the front-panel complexity would be much greater, requiring 330 separate keys to select and control all of the features available in the HP 3577A. When a user presses one of the front-panel keys, the appropriate menu of softkey labels is displayed along the right side of the display. The desired softkey function can then be selected by using the pushbutton switches that are an integral part of the display bezel. An extensive softkey approach can be intimidating if several levels of nesting are used, so most menus on the analyzer use only one level of nesting (i.e., pressing a front-panel key brings up only one menu, with no underlying second level of softkeys). The menu hierarchy is very regular, with similar features being accessed in a consistent manner.

Display of Data

The display used in the HP 3577A is the HP 1345A Graphics Display.[1] This is a high-resolution (2048×2048 points) vector display. The user also has access to the HP 1345A Display and can directly enter annotation, softkey labels, and graphics. The ability to read the keyboard remotely and a full HP-IB service request capability allow the HP 3577A to act as the user interface in an automated test system.

The basic measurements made by the HP 3577A are amplitude and phase. However, the actual measurements displayed can be more complex. The input selection can be as simple as **INPUT A**, **B**, or **R**, or it can be a ratio such as A/R or a very complex equation containing input channels, constants, and other functions.

The Y-axis information can be displayed as the log magnitude, linear magnitude, phase, polar, real part, imaginary part, or group delay of the input selection. The Y-axis format is selected by choosing the appropriate softkey function in the menu obtained by pressing the **DISPLY FCTN** key in the front panel's Display Format section. The LIN MAG function is useful when a display of a device's gain or loss is desired. PHASE gives a display of the phase shift through the device under test. POLAR provides a linear display with the horizontal axis being the real part of the measurement and the vertical axis being the imaginary part of the measurement. The resulting plot then is the locus of real and imaginary data as the selected frequency range is swept. This type of display is particularly useful when measuring the reflection characteristic of a device. The REAL and IMAG-

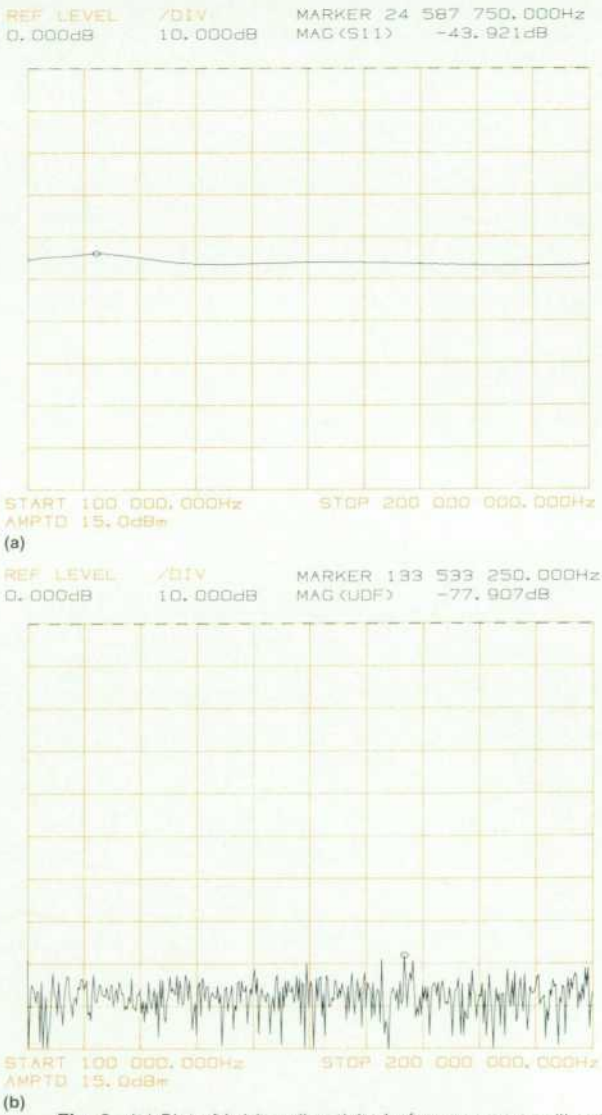

Fig. 2. *(a) Plot of bridge directivity before one-port calibration. (b) Plot after one-port calibration.*

inary functions are valuable when the input selection is chosen so that the direct measurement of impedance can be displayed. Thus, the real and imaginary parts of the impedance parameter can be viewed versus frequency. The important group delay parameter is also available via the DELAY softkey display function. Group delay is the derivative of the measured phase with respect to frequency.

In addition to the flexible control of the Y-axis display of data, the HP 3577A has several types of X-axis control. The features available in the softkey menu obtained by pressing the **SWEEP TYPE** key in the Source section of the front panel include linear frequency sweep, alternate sweep, logarithmic frequency sweep, continuous wave, and sweep direction. Pressing the LIN FREQ SWEEP softkey selects a linear, phase-continuous sweep from a user-specified start frequency to a user-specified stop frequency. ALTERNTE SWEEP allows two totally different linear X-axis sweeps to occur. The first trace is swept first over its frequency definition and then the second trace can be swept over an entirely independent frequency definition. Both traces can be displayed at the same time. For example, this sweep definition can allow the simultaneous display of the passband and the stopband characteristics of a filter.

The HP 3577A can perform a logarithmic frequency sweep from an arbitrary start frequency to an arbitrary stop frequency. This feature can be used to display traditional Bode plots of the frequency response of networks. CW (continuous-wave) sweeps are useful for repeatedly taking data at the same frequency. Many computer-based instrument systems can use this mode to take data rapidly at many different specified frequencies. The frequency sweep direction (up or down) for the linear sweeps can be varied to suit the measurement needs of the user.

Another significant feature of the HP 3577A is the ability to select the delay aperture. The delay aperture is defined as the change in frequency over which the change in phase is calculated. The ability to select this parameter allows the user to make important trade-offs between delay resolution and noise.

The wide dynamic range of the instrument and the versatile display formatting often cause the measured data to be limited at the top or bottom of the display. When this occurs, the AUTO SCALE softkey provides the user a quick way of getting all of the data on the display. The automatically scaled display may not be exactly what the user wants to see, but it is usually close and always puts the data on the screen.

Measurement Features

Data Storage. Data from the HP 3577A's three receivers is in complex vector form to retain both magnitude and phase information. This data can be stored and later recalled and redisplayed in whatever display function the user requires regardless of what display selection was made when the data was stored. The data is stored in floating-point format, which retains the full accuracy of the HP 3577A regardless of what scale parameters were used at the time the data was taken. The data memory in the analyzer is nonvolatile so that a power failure will not destroy stored data.

Normalization. The HP 3577A's normalization function provides a simple means of canceling source and receiver accuracy and flatness errors, test fixture errors, and cabling errors (both magnitude and phase). For a transmission measurement, the user removes the device under test (DUT) and replaces it with a through connection. Pressing the NORMLIZE softkey stores the remaining magnitude and phase errors. The DUT is then reinserted and all measurements are made relative to the stored error data. The use of digital storage and a high-stability circuit design allow very precise measurements. Previous instruments required an additional accessory to perform this calibration.

The one-port calibration feature goes one step further by providing a means of canceling the errors inherent in a return-loss bridge. During calibration, the user is prompted

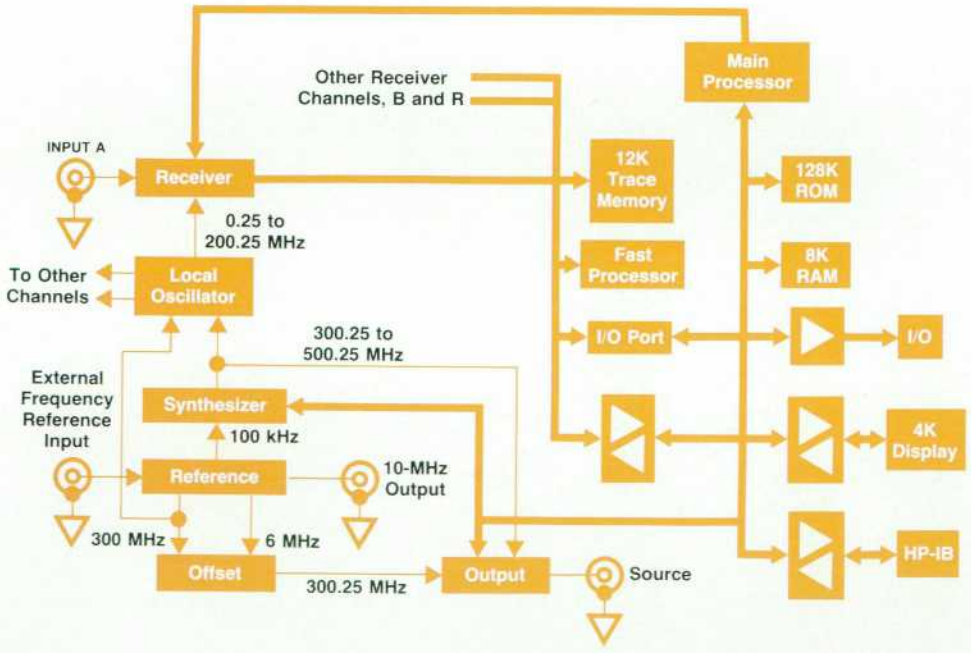

Fig. 3. *Simplified block diagram of the HP 3577A Network Analyzer.*

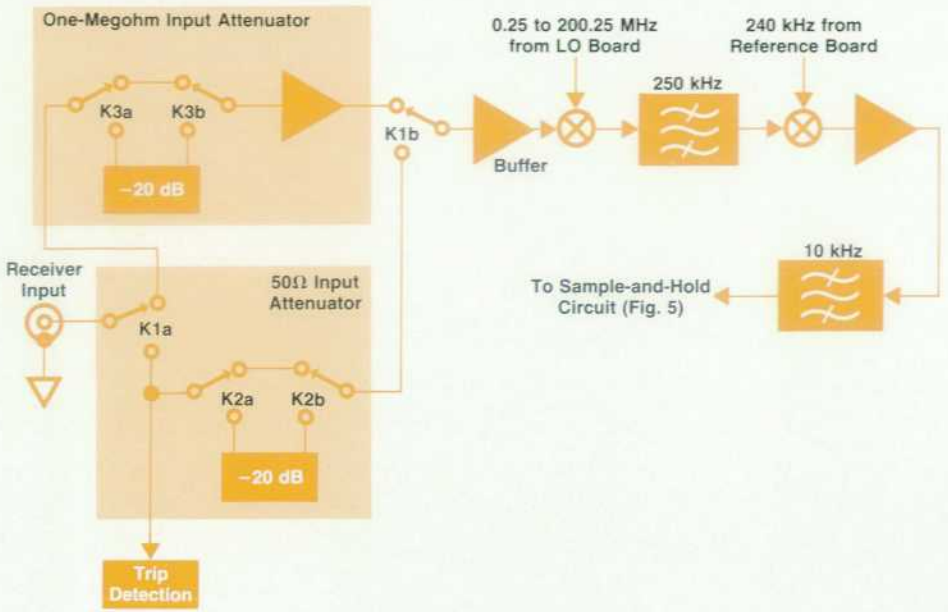

Fig. 4. *Block diagram of the input impedance paths for each of the HP 3577A's receivers.*

to connect, in turn, an open circuit, a short circuit, and a reference load to the test port. The HP 3577A automatically records the data associated with each of these and configures itself for a three-term corrected reflection measurement. A slightly less accurate two-term correction is also available that requires only an open circuit and a reference load. The one-port error correction can improve the directivity of a typical bridge from 40 dB to an effective directivity of 75 dB (see Fig. 2).

Noise Averaging. Since the input data is stored as complex vectors, incoherent noise can be reduced by averaging the data from the current sweep with data from previous sweeps. The data is weighted exponentially with the most recent data weighted the most and the oldest data weighted the least. This results in a fast, memory-efficient algorithm that reduces noise while still responding to a drift in the data. The exponential averaging factor must be a power of two and can be selected via the softkey menu. This form of averaging should not be confused with video filtering, which only estimates or smooths the noise.

Vector Math. The HP 3577A's vector math capability allows the user to define functions that are themselves mathematical expressions consisting of other functions, stored data, constants, and input data. To simplify function definition, the HP 3577A has several useful built-in expressions (closed-loop-to-open-loop response, normalized impedance, and impedance) which can be used directly or can be modified by the user. A user can display the input characteristics of a device in S-parameter form (reflection coefficient) or use the vector math features to convert the reflection coefficient to input impedance. Depending on what display function is selected, the magnitude, phase, real part, or imaginary part of the impedance can be shown (see box on page 8 for some examples). The impedance can also be shown in polar form, which provides both amplitude and phase information on the same trace.

Devices under test often have significant delay in their transmission paths, which causes large amounts of linear phase shift. The absolute value of the delay may not be meaningful, but the deviation from linear phase (or pure delay) is often important, especially in digital systems. The PHASE SLOPE softkey allows the user to add or subtract up

(continued on page 9)

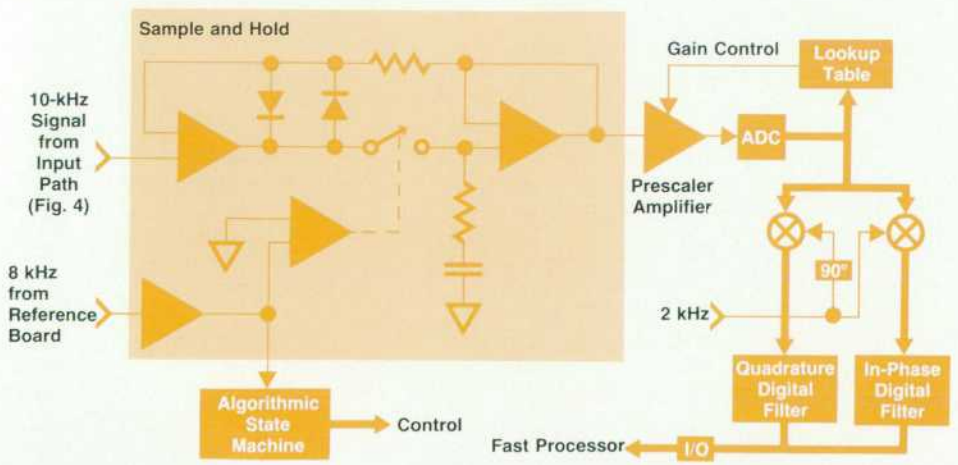

Fig. 5. *Input signal processing section of the HP 3577A's receivers.*

User-Defined Vector Math Expands Measurement Capabilities

The HP 3577A Analyzer's vector math capabilities not only increase its power in traditional network analysis, but also extend its usefulness to less-traditional measurement areas. In contrast to the trace math functions of earlier analyzers, which simply manipulate an instrument's display, vector math performs complex calculations involving the actual measured data. The results are then displayed and can be scaled in virtually any form the user desires.

The measurement of quartz crystal parameters provides an excellent example of vector math at work. Traditionally based on complex impedance measurements, these parameters have long been a difficult measurement problem. Vector impedance meters are commonly available, but no single unit has ever combined the necessary frequency coverage (up to 200 MHz), frequency resolution (0.01 ppm), and measurement accuracy (±0.02 dB) for these devices. While the HP 3577A is primarily a network analyzer, it can furnish these impedance meter functions easily by means of its vector math capabilities.

Fig. 1 shows the reflection coefficient (s_{11}) of a quartz crystal in the vicinity of series resonance. This traditional network measurement is defined as the ratio of the power reflected from a device to that supplied to it. In this case, the HP 3577A measures the reflected signal in its **A** receiver and the incident signal in its **R** receiver. Reflection coefficient is calculated as A/R and displayed here as magnitude and phase versus frequency.

Transmission-line theory indicates that for every value of reflection coefficient there is a corresponding value of normalized impedance Z_x/Z_o, where Z_x is the device impedance and Z_o is the system impedance. In other words, after measuring s_{11} for a given device, its impedance can be calculated from.

$$Z_x = Z_o(1+s_{11})/(1-s_{11})$$

With the HP 3577A's vector math capability, this calculation can be performed automatically for each point of the measurement sweep as it is taken, yielding the real-time impedance display

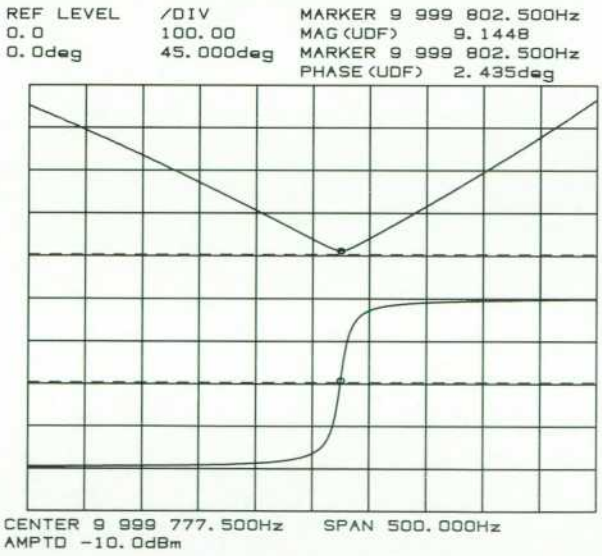

Fig. 1. *Magnitude (top curve) and phase (bottom curve) of the reflection coefficient s_{11} of a quartz crystal near its series-resonant frequency.*

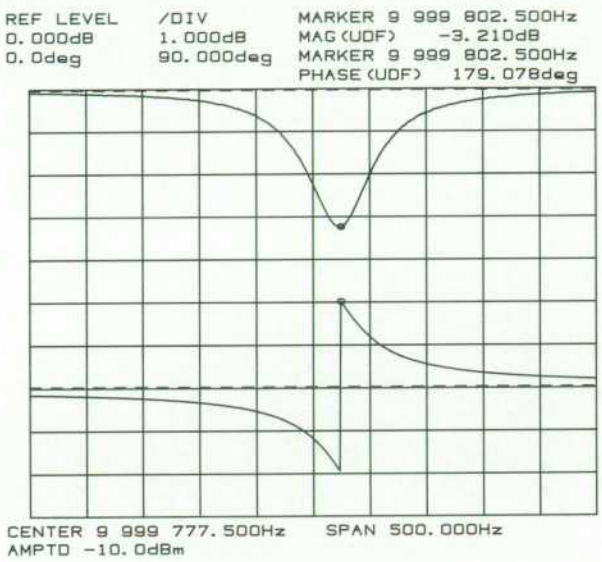

Fig. 2. *Magnitude (top curve) and phase (bottom curve) of the crystal impedance, as calculated from s_{11} using the HP 3577A's user-defined vector math capability.*

of Fig. 2.

Operation is simple. On the softkey menu obtained by pressing the instrument's **INPUT** key, the original selection of A/R corresponds to s_{11}. By pressing the USER DEFined INPUT softkey, the operator is prompted to enter symbols corresponding to an input expression of the operator's choice. In this case the expression is:

$$K2*(K1+A/R)/(K1-A/R)$$

where the arbitrary constants K1 and K2 are assigned values of 1 and 50, respectively.

This transformation from s_{11} to complex impedance is useful enough that the above equation is predefined for the HP 3577A user upon instrument turn-on or preset. All that need be done is to select special function F4 via the same user-defined input menu. Combined with the instrument's internal calibration firmware and a set of accurate impedance standards, impedance measurements of very satisfactory accuracy and repeatability are thus obtained.

However, this does not yet solve the entire crystal measurement problem. From the crystal's equivalent circuit diagram (Fig. 3) it can be seen that a shunt capacitance C_o is modeled across the series, or motional components R1, L1, and C1. Away from resonance, the motional arm presents a fairly high shunt impedance, isolating C_o for measurement via conventional techniques. Near resonance, however, the reactance of C_o distorts the apparent impedance of the motional components, making their values difficult to determine.

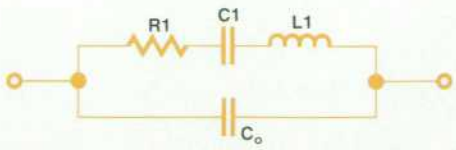

Fig. 3. *Equivalent circuit model of a quartz crystal device.*

Again calling upon vector math, the reactance of C_o can be mathematically removed from the overall impedance plot. To do so, specify a user-defined input expression of:

$$(K3*F4)/(K3-F4),$$

where F4 is the calculated crystal impedance function previously described and K3 is a complex constant representing the impedance of C_o. Use the **DEFINE MATH** softkey menu to assign to K3 a value of $0-jX_o$, where X_o is the calculated reactance of C_o at the crystal's resonant frequency (X_o can be safely approximated as frequency-independent over the very small frequency spans used for crystal measurements).

These calculations accomplished, the display will now show the crystal's impedance as if C_o were not present; that is, as a simple series-resonant circuit composed of the motional components R1, L1, and C1. At series resonance (identified by the phase zero crossing) the total crystal impedance is simply R1. The slope of the reactance at phase zero crossing yields values for L1 and C1, and crystal Q can be calculated from phase variations with frequency.

User-defined vector math allows the HP 3577A to perform these functions without an external computer. Despite its birthright as a general-purpose test instrument, it is able to duplicate or surpass functions formerly found only in more specialized equipment.

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Product Marketing Engineer
Lake Stevens Instrument Division

to 72,000 degrees per span of linear phase shift to or from the phase display so the user can measure the deviations from a linear phase response.

Hard Copy

To provide some sort of permanent hard copy of the data, the HP 3577A Analyzer supports direct dump of the display via the HP-IB to listen-only, HP-GL plotters. The analyzer is configured as a talk-only HP-IB device, so no external HP-IB controller is required. The firmware supports complete dumps of the display and allows selective plots so that several traces can be plotted on one graticule. Selectable pen number, pen speed, and line type allow the user to customize the plot. Positioning the marker where desired on the display and pressing the PLOT MARKER softkey lets the user record high-precision readings at multiple points on the plot. Fig. 2 shows two plot examples.

Data Transfer

The HP 3577A provides access to all of its data storage via the HP-IB and can dump and load data in three different formats:

- An ASCII format that can be used by most computers
- A 64-bit floating-point format directly compatible with HP 9000 Series 200 Computers and allowing faster total measurement times since no data translation is needed
- An internal HP 3577A format that can be used for temporary storage of data by an external computer system.

S-Parameter Test Sets

S-parameter (scattering matrix) measurements represent the industry standard for the characterization of N-port networks, including active and passive devices, for frequencies extending from approximately 100 kHz through 100 GHz and beyond. The HP 35677A/B S-Parameter Test Sets (for 50Ω and 75Ω systems, respectively) were developed to provide this capability for two-port S-parameter measurements with the HP 3577A, covering a frequency range from 100 kHz to 200 MHz (the upper frequency limit of the HP 3577A). The test set implementation is based on the standard reflectometer bridge design that has been used for many years by Hewlett-Packard. Duplication of overhead circuitry was avoided by deriving all power and control functions from the HP 3577A. A simple four-wire interconnect provides these power and control functions, resulting in a very cost-effective, high-performance instrument that complements and extends the functional capabilities of the HP 3577A. (See article on page 17 for more details about the HP 35677A/B Test Sets.)

Hardware Design

Fig. 3 shows the functional blocks making up the HP 3577A. The source produces the synthesized 5-Hz-to-200-MHz stimulus for a device or network under test. The source also generates the frequency sweep and controls the output amplitude from 15 dBm to −49 dBm in 0.1-dB increments. Each of the three identical receivers tracks the

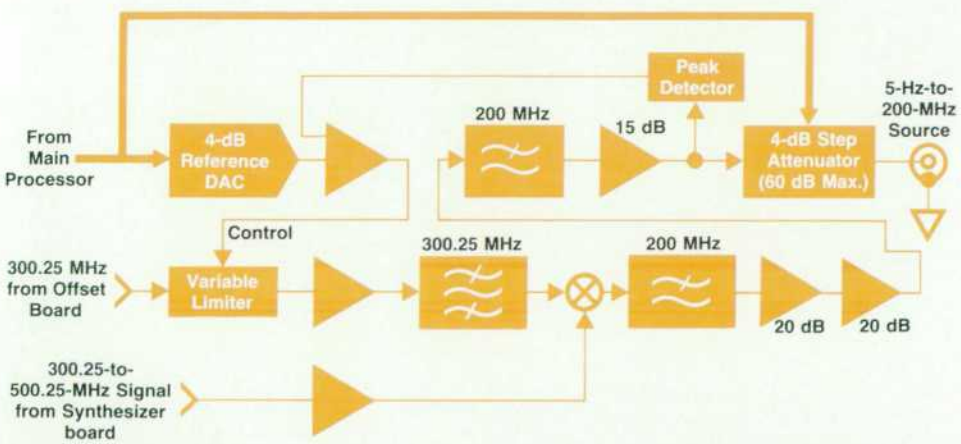


Fig. 6. *Block diagram of the output board.*

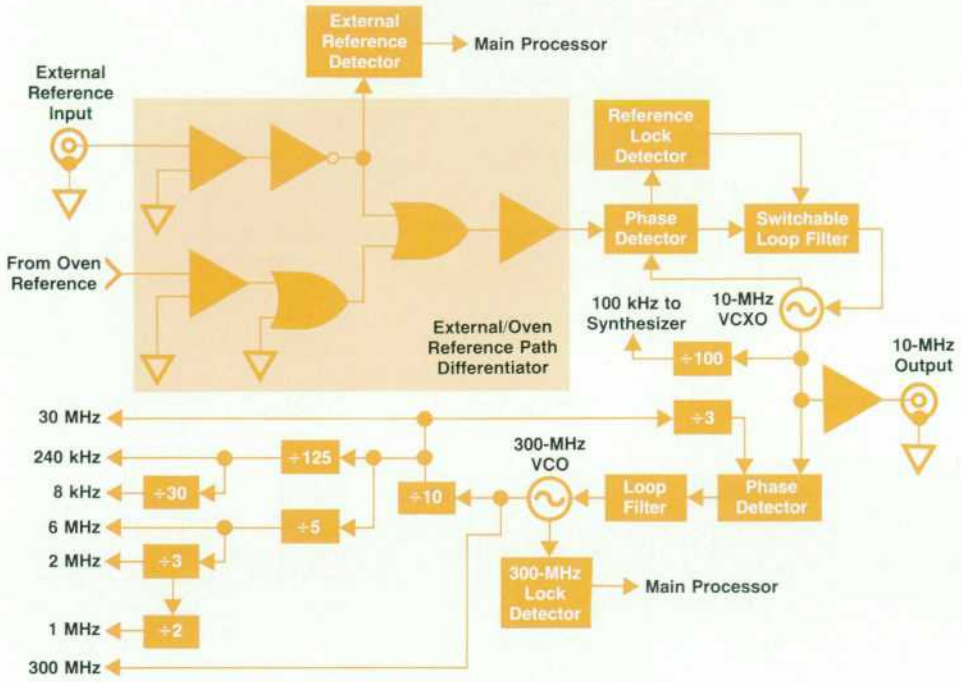


Fig. 7. *Block diagram of the frequency reference board.*

source frequency and measures the real and imaginary parts of the signal coming into its input (usually from the output of the DUT). A very fast vector math processor takes the real and imaginary data from each of the receivers, saves this raw data in memory, and converts it to the selected display function. The main processor provides the user interface, controls the internal circuits, services the HP-IB, and updates the display of data on the CRT.

Receiver. The block diagram shown in Fig. 4 illustrates the conversion of the input impedance paths for different measurement requirements. The input signal to the receiver section is translated in frequency and filtered using all analog processing. In the one-megohm input position the input signal goes through a one-megohm, 0-to-20-dB attenuator. In the 50Ω input position a higher frequency response is possible. An overload detector measures the signal level at the input to the 50Ω attenuator and if a damage-level signal is present, the input relay trips and automatically selects the one-megohm input position. A message is then sent to the CRT display to indicate what has happened and to explain how to reconnect to the 50Ω input position.

After the input attenuator, the signal goes through a unity-gain buffer amplifier to the first mixer for down-conversion. The first mixer is a diode and transformer double-balanced mixer. The local oscillator (LO) drive signal is a 7-dBm tracking signal that is tuned to 250 kHz above the input frequency. Thus, the frequency range of the LO is 250 kHz to 200.25 MHz. The output of the mixer is a constant 250-kHz IF. Following the mixer is a 250-kHz bandpass filter that has a zero at 230 kHz, the image frequency for the second mixer. The second mixer is a transistor array with an LO drive of 240 kHz. The 250-kHz and 240-kHz signals mix to provide the 10-kHz IF, which is then amplified to levels that provide an optimum signal-to-noise ratio for the active 10-kHz bandpass filter.

The purpose of this 10-kHz bandpass filter is to provide an antialiasing filter of approximately 1.7-kHz bandwidth. This bandpass filter is a cascade of six active second-order RC sections. Two of these sections have a transmission zero at 14 kHz. This zero is necessary to reject any signal

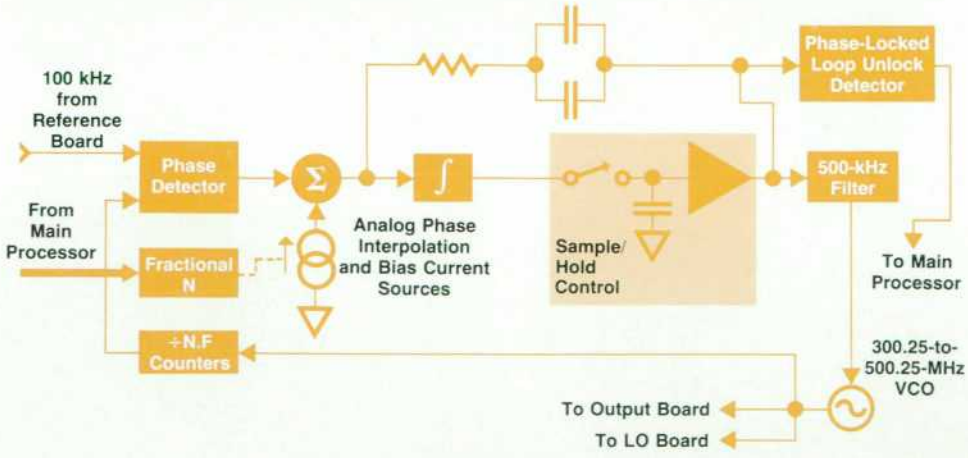


Fig. 8. *Block diagram of the synthesizer board.*

aliasing with the second harmonic of the 8-kHz sampling frequency used in the following sample-and-hold circuit (Fig. 5). Also included in the 10-kHz bandpass filter is an all-pass network stage that provides a means of adjusting the phase shift through the filter. The sequence in which the second-order sections are cascaded is optimized for the best noise performance.

The 10-kHz signal is sampled at an 8-kHz rate with a sample-and-hold circuit (see Fig. 5). At first glance it might appear that sampling a 10-kHz signal at 8 kHz violates the Nyquist criteria for sampling. However, what is really happening is that a bandwidth of 1.7 kHz is sampled at 8 kHz. The information at 10 kHz can be thought of as being translated in frequency from 10 kHz to 2 kHz just the same as if it had been down-converted in a mixer.

The sampled signal is then converted from an analog signal to a digital sequence by an analog-to-digital converter (ADC), which is an 8/12-bit successive-approximation IC. One of the contributions of the total A-to-D process is the prescaling variable-gain amplifier in front of the ADC. The converter operates in a two-pass operation. On the first pass, the prescaling amplifier is set to a gain of 1.1 and an 8-bit conversion is made. This output is processed by a state machine and a number is fed back to program the prescaling amplifier to the gain required to get the signal to approximately a full-scale level. The second-pass conversion is then done to 12-bit resolution. The results of the two conversions are combined to produce a 26-bit word. The extra bits are used by internal arithmetic processing steps and then truncated from the result.

This two-pass conversion approach provides not only 12-bit resolution at full scale, but 12-bit resolution all the way down to 42 dB below full scale.

The ability to take two conversions and put the results together to form a useful answer is made possible by an accurate tantalum-nitride resistor network with a ratio accuracy of better than 0.02%. These resistors are used as part of the variable-gain amplifier. (For a discussion of the design of this ADC, see article on page 21.)

The output of the ADC is a digital sequence representing a 2-kHz signal. This output contains both the amplitude and phase information of the signal coming into the receiver input. Quadrature detection is used to extract the required amplitude and phase data. The digital sequence representing the 2-kHz signal is applied to two digital mixers simultaneously. One mixer uses a local oscillator that generates a digital sequence representing a sampled cosine function. The other mixer uses samples of a sine function. The results of this mixing process are two data streams, one representing the real part of the input signal and the other representing its imaginary part.

The two data streams are filtered separately by custom digital filters that define the instrument's resolution bandwidth (1 Hz, 10 Hz, 100 Hz, and 1 kHz). The filters are four-pole Bessel filters implemented as custom integrated circuits. These variable-bandwidth filters allow the accurate measurement of devices with steep frequency responses and help reduce the measurement noise. The output of each filter is a 24-bit two's-complement number. The 24-bit numbers representing the real and imaginary parts of the input signal are then sent to the fast vector math processor for further manipulation into functions such as magnitude and phase.

Source. The source output (Fig. 6) is generated by mixing a 300.25-MHz signal from the offset section with a signal from the 300.25-to-500.25-MHz synthesizer. The result is a 5-Hz-to-200-MHz source output frequency. The output mixer is a double-balanced diode ring mixer. The LO level is 15 dBm. The 300.25-MHz signal at the RF port of the mixer is varied over an approximate 10-dB range by using another double-balanced mixer as a variable limiter. This limiter is switched at a high level and its output is controlled by a current summed into its dc port. The output signal is then filtered by a 200-MHz low-pass filter to eliminate out-of-band responses before it is amplified by two identical amplifier stages. These 20-dB stages have very flat frequency response from 1 Hz to greater than 200 MHz and are designed as complementary amplifiers with local feedback to obtain optimum biasing.

A second 200-MHz filter is used before the final 15-dB power stage, which is used to provide the 15-dBm signal at up to 200 MHz. This amplifier is also a complementary design to optimize for low distortion. A dc servo loop (not shown in Fig. 6) is built around the entire amplifier chain to keep the output coupled at ac only; that is, to maintain the dc level of the output at reference ground. The output amplifier maintains its ac level by using a peak detector to sense the output and provide a feedback signal to correct the amplitude. The frequency response below 100 kHz is flat enough that leveling is not necessary. The synthesizer controls a signal that tells the main processor whether or not to level the output board. This signal can be sent even during a sweep so that leveling can be enabled or disabled dynamically.

The level of the output signal is controlled over a 4-dB range in 0.1-dB steps by using a digital-to-analog converter (DAC) to set the reference voltage level for the variable limiter. Amplitude sweeps are accomplished by having the HP 3577A's main processor continuously send out new amplitude settings for this DAC. Further control of the

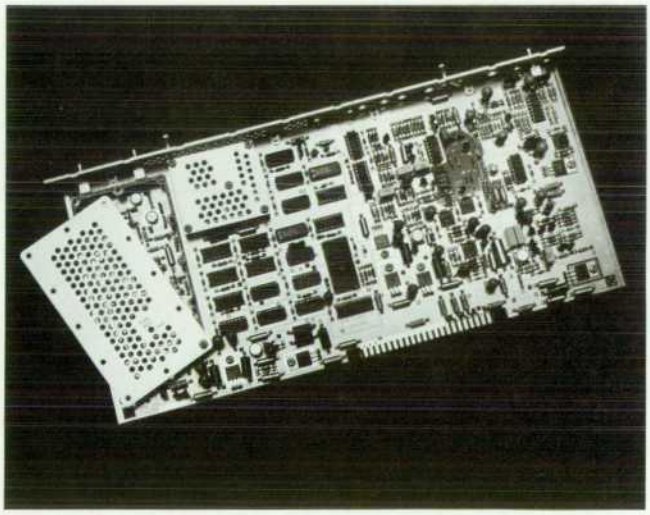


Fig. 9. *Photograph of the synthesizer board showing RF shielding cans.*

output level is provided by a 60-dB attenuator which is constructed in 4-dB steps. The 4-dB pads are switched using high-reliability RF relays.

Frequency Reference. The frequency reference circuitry (Fig. 7) generates signals synthesized from one common reference frequency. The main reference frequency is automatically selected from either the internal 10-MHz coarse crystal oscillator, the internal 10-MHz high-stability oven oscillator, or a user-supplied external reference of 10 MHz/N where N can be any integer from 1 to 100. The hierarchy of selection is external reference first, oven oscillator second, and finally coarse 10 MHz. If none of the above selections achieves a phase-lock condition, an Oscillator Unlocked message is displayed by the processor. The selected 10-MHz reference frequency is used to lock an internal 300-MHz VCO. All of the other fixed frequencies needed by the HP 3577A's circuits are generated by dividing down from the 10-MHz and the 300-MHz signals.

Fig. 7 illustrates how the coarse 10-MHz VCXO and the alternate references are interfaced with the 300-MHz oscillator. The external reference and the internal oven reference are buffered by comparators and applied to an OR gate. The presence of the external reference signal is sensed by a detector; if the signal is present, a shutdown signal is sent back to the oven oscillator to switch off its output. The output of the OR gate is used to generate a pulse that will provide an input into the phase detector of the 10-MHz phase-locked loop. If an external reference is not present and the oven oscillator has not yet stabilized (a condition that can exist just after the HP 3577A is turned on), the coarse 10-MHz VCXO controls the loop.

The output of the 10-MHz phase-locked loop is used for several purposes:

- It is supplied to the user for locking other instruments to a common reference. This signal has the advantage of being "cleaned up" in terms of phase noise by the loop bandwidth of 3 Hz.
- It is sent to the HP-IB interface board.
- It is divided by 100 to obtain the 100-kHz frequency reference that is used by the fractional-N synthesizer.
- It is also used as a reference for the 300-MHz phase-locked loop.

The circuit configuration used for the 300-MHz VCO is used in several of the circuit blocks in the HP 3577A. This configuration is called a negative-resistance oscillator. It makes use of the property that the input impedance of a common-base transistor circuit with inductance in the base lead is negative over some range of frequencies. A tuned circuit placed in parallel with this negative impedance will result in sustained oscillation. The inductor for the tuned circuit is implemented by using a section of short-circuited semirigid coaxial cable. The VCO is tuned using voltage-variable diode capacitors in the tuned circuit. The output of the 300-MHz oscillator is used by the LO circuitry and the offset frequency loop. A divided-down 30-MHz signal is used to provide a clock for the fast processor.

Other frequencies generated by the reference circuitry are 6 MHz, 2 MHz, 1 MHz, 240 kHz, and 8 kHz. The 240-kHz and 8-kHz outputs are used by the receiver board for the down-conversion LO and sampling signals, respectively.

Synthesizer. The synthesizer board (Fig. 8) generates a 300.25-to-500.25-MHz frequency with 0.001-Hz resolution and can be swept in a phase-continuous fashion over the entire 200-MHz span. The output from this board is used to provide the sweeping signal for both the source output and the tracking receiver LO.

The basic synthesis technique is fractional-N frequency synthesis.[2] This technique for synthesizing frequencies of arbitrary resolution uses a phase-locked loop, a divide-by-N counter, a "pulse swallowing" variable modulus counter, and analog circuitry to correct for phase interpolation. A proprietary IC and a custom resistor network are used to realize the performance and cost advantages of this technique.

Several circuit improvements have been added to enable fractional-N frequency synthesis to be performed at frequencies of 300 to 500 MHz. Advances in operational amplifier technology have allowed discrete circuits to be replaced with high-performance ICs. One example of this is the integrator shown in Fig. 8. A 500-kHz low-pass filter after the sample-and-hold circuits filters out the high harmonics of the 100-kHz reference frequency used by the phase-locked loop. This prevents these signals from becoming phase sidebands on the output. A major contribution is the ability to sweep the entire frequency range in one band. The VCO that provides this capability is similar to the 300-MHz oscillator design described earlier. It is a negative-impedance oscillator using a shorted transmission line as an inductor and varicap diodes as the tuning elements. The ability to obtain a negative resistance region over such a large frequency range required careful optimization of several parameters. Many of the performance characteristics were achieved only after design attention was focused on good RF shielding techniques. Fig. 9 illustrates the shielding used to minimize coupling between circuits on the synthesizer board and circuits on other boards.

250-kHz Offset. The HP 3577A's design requires generation of an offset frequency equal to the receiver IF. The source and the receivers therefore are tuned to the same frequency as they are swept from 5 Hz to 200 MHz. A 250-kHz refer-

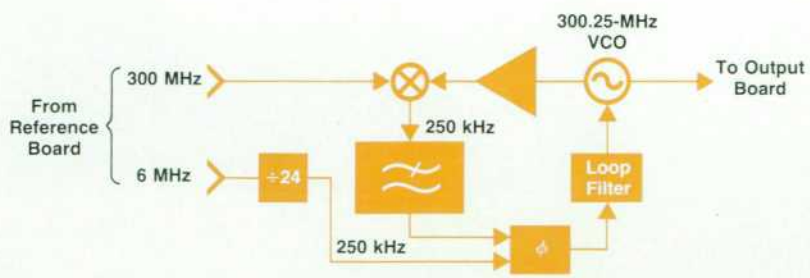


Fig. 10. *Block diagram of the offset frequency board.*

ence is obtained by dividing the 6-MHz output from the frequency reference board by 24. This frequency is used as one input to a phase detector that is part of the phase-locked loop of the offset board (Fig. 10). The 6-MHz and 300-MHz outputs from the frequency reference board are sent to the offset board, which generates a 300.25-MHz signal that is sent to the output board to mix with the 300.25-to-500.25-MHz swept LO. The 300.25-MHz VCO is another negative-impedance design. This oscillator's output is mixed against the 300-MHz synthesized reference signal and the lower sideband of 250 kHz is then compared with the 250-kHz reference signal in a phase detector. The dc signal out of this phase detector is used to control the 300.25-MHz phase-locked loop whose output is the desired 250-kHz offset frequency synchronized with the reference.

Local Oscillator. The local oscillator board (Fig. 11) appears to have a deceptively simple function. The circuit is designed to provide three identical 0.25-to-200.25-MHz tracking LO signals for the HP 3577A's three receivers. The tracking signals are produced by mixing a fixed 300-MHz signal from the reference board with the swept 300.25-to-500.25-MHz output from the synthesizer. There are several important performance characteristics that require special attention. The three LO signals must be matched in phase and amplitude (although amplitude matching is of lesser consequence) over a 200-MHz bandwidth. There are several types of spurious responses that, if present, would be converted by the mixers on the receiver board and produce dynamic range limitations. Hence, the requirement for the dynamic range of the receivers to be better than 100 dB places some severe constraints on the LO signal purity.

The required level of performance of the local oscillator board was achieved by careful design of the filters, mixers, and shielding, and by using a limiter for single-sideband rejection. Various 200-MHz and 300-MHz low-pass filters are used to ensure pure signal inputs to amplifiers and mixers. The main conversion mixer used to generate the 0.25-to-200.25-MHz output is a high-level, double-balanced mixer capable of providing low-level, high-order mixer products. Special RF shielding cans and circuit placement are used to obtain the high on-board frequency isolation (over 120 dB at several hundred MHz).

A typical mixer used for frequency translation has several undesirable conversion mechanisms. One such mechanism is single-sideband detection of signals on the switching port. It is important, therefore, that the level of single-sideband signal delivered to the mixer be reduced to an acceptable range. The local oscillator board uses a limiter in the signal path to control the level. It is well known that a single-sideband signal can be modeled as a sum of an amplitude-modulated signal and a phase-modulated signal. The limiter converts any single-sideband level to a phase-modulated double-sideband signal by removing any amplitude modulation. The particular type of limiter chosen (the mixer-limiter configuration) also has the advantage of providing feedback around the limiter, which further stabilizes the output against frequency response losses.

Oven Reference. The oven board provides the 10-MHz high-stability crystal oscillator reference frequency for the HP 3577A. For high-stability operation while the temperature of the oven is reaching a stable point, the user can supply an external 10-MHz oscillator. Otherwise, the HP 3577A uses its coarse 10-MHz VCO as a reference until the oven source stabilizes.

As the HP 3577A warms up to a constant temperature, the current flowing into the oven is monitored. During the warm-up period the required current is greater than the current required later to keep the oven at a stabilized temperature. The decrease in this current is measured and used to enable an output switch that delivers the 10-MHz oven reference signal to the reference board. This RF switch can also be enabled/disabled by a signal from the reference board that indicates whether an external 10-MHz reference is present (see Fig. 7). The RF switch consists of a transistor and two FETs that together provide at least 100-dB rejection of the 10-MHz signal when the switch is off.

Power Supply. The power supply for the HP 3577A is a switching regulator design which has good efficiency. The configuration used is referred to as a half bridge. The ac power line voltage is rectified to form a dc voltage that is switched at a 40-kHz rate by MOSFET switches to provide the signal to be transformed to the desired secondary voltages. The feedback control is around the rectified 5V secondary output. The error voltage is supplied to a pulse width modulator IC for loop correction.

One interesting outcome of developing an instrument-quality switching power supply is that a large portion of the cost and a lot of the design and development time was spent on providing protection circuits for the supply. Some of these circuits enable the supply to withstand accidental abuse and some allow the supply to be relatively insensitive to power line variations. The HP 3577A's power supply is designed to withstand a range of line voltages as well as instantaneous excessive voltages (surges) and instantaneous excessively low voltages (sags). Whenever an out-of-tolerance line voltage exists for a substantial time, the supply shuts down in an orderly fashion. This means that the RAM portion of the microprocessor is disabled before its 5V power is removed. The supply is also internally protected against accidental servicing abuses and component failures. The supply shuts down in case of secondary overvoltages and current limits, primary current limits, and excessive environmental temperatures.

A switching power supply can be thought of as a time-

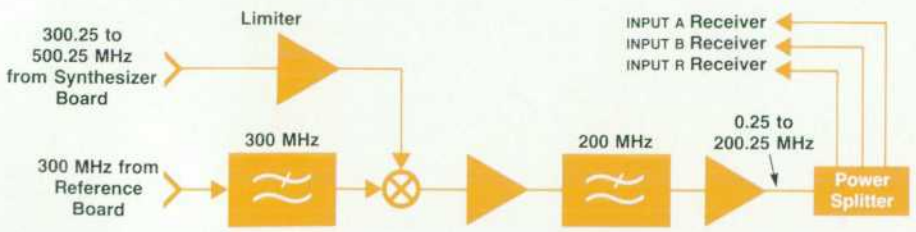


Fig. 11. *Block diagram of the local oscillator (LO) board.*

varying linear system. Closing the feedback loop from the 5V dc output to the pulse width modulator chip is a control loop problem. Designers usually want a great deal of gain to reduce ripple at the input frequencies and, for loop stability, want to have gain crossover determined by a single pole. These conditions, along with the requirement of a two-pole filter for reducing the switching frequency to a low level, make for interesting design challenges. Some solutions for reducing the two-pole rolloff to a single-pole rolloff use the inherent equivalent series resistance that occurs in the capacitor used for switching frequency filtering. This resistance can provide a zero that can aid the loop response shaping. While this type of loop compensation can be used successfully, it does depend on an often unspecified and uncontrollable parameter—the filter capacitor's ESR or equivalent series resistance.

The power supply in the HP 3577A was designed using a different two-loop technique to provide frequency compensation for the switcher. One feedback loop, the inner or ac loop, senses the 40-kHz output before the LC section of the 40-kHz filter. The outer or dc loop senses the dc output after the conversion to 5V has taken place. The two loops are then summed for a common error signal. One advantage of this scheme is that the poles of the inner loop become zeros in the overall feedback response equation. Thus, a properly placed pole in the inner loop can become a zero that compensates for the LC filter rolloff. This gives a very important degree of freedom for the control loop design. In addition, the compensation is very well controlled and can be accurately used to provide the required level of stability.

Digital System

The digital processing capabilities of the HP 3577A are provided by two separate microprocessors (see Fig. 3). The main processor is an MC68000 and its partner, the fast processor, is a 2900-family bit-slice processor that is microprogrammed to do the real-time data processing in the instrument. The main processor handles the user interface, HP-IB protocol, analog hardware control, and service diagnostics. It also provides a list of tasks for the fast processor to perform during every frequency sweep. The trace memory provides 24K bytes of nonvolatile storage, which is accessible by both the main processor and the fast processor. The main processor RAM and the trace memory RAM consist of low-power CMOS devices that are automatically powered by a lithium battery when ac line power is not applied to the instrument.

The fast processor is made up of four 2901 bit-slice ALU chips, each four bits wide, resulting in a 16-bit wide data path. The microcode resides in a 2K×48-bit ROM array and provides all of the control signals for the fast processor. A 2910 microsequencer chip combines instructions from the microstore with conditions in the ALU to provide conditional and unconditional branching and subroutine calls. Most of the fast processor is implemented using high-speed Schottky-technology parts.

Although the analyzer provides a phase-continuous frequency sweep, data is taken and stored at discrete points, typically 401 points per sweep. On a point-by-point basis, the fast processor takes the data from the three receivers, multiplies it by a gain factor, adjusts the phase for any electrical length compensation, performs the vector averaging algorithm, and stores the corrected data in trace memory. The data from the three receivers is of the form R + jX, where R is the real or in-phase portion of the vector and X is the imaginary or quadrature portion of the vector.

The fast processor then processes the data according to the functions selected and/or defined by the user. After the fast processor completes its signal processing tasks it scales the data for the display and passes the data to the main processor. The main processor takes the data on an interrupt basis and writes it to the memory of the internal HP 1345A Display (with optional memory board), which provides high-quality vector graphics.

The HP-IB interface is implemented using a TMS9914A interface IC under the control of the main processor firmware.

Trace Math

Vector averaging is performed using the following algorithm:

$$R_{avg} = (1/k)R_{new} + R_{acc}[(k - 1)/k]$$

$$\text{and } X_{avg} = (1/k)X_{new} + X_{acc}[(k-1)/k]$$

where R_{acc} and X_{acc} are the accumulated values from previous sweeps, R_{new} and X_{new} are the values from the current sweep, and k is the averaging constant selected by the user (either 1, 2, 4, 8, 16, 32, 64, 128, or 256). This algorithm results in the data from previous sweeps being averaged according to an exponential weighting, with the most recent sweeps weighted the most. Thus, the algorithm can follow drifts in the data while still providing a reduction in the variance. Restricting k to powers of two makes the averaging calculations significantly faster, since in floating-point notation incrementing or decrementing the exponent

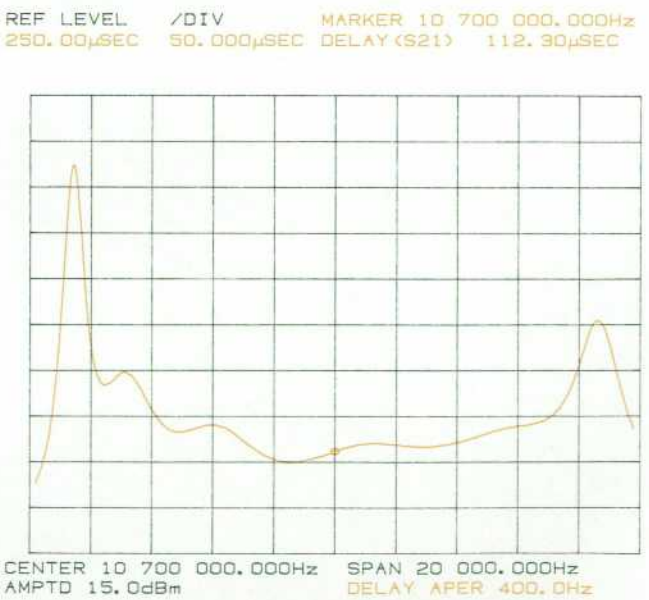


Fig. 12. *Plot of group delay as measured by the HP 3577A.*

is equivalent to a multiply or divide by two. To facilitate efficient start-up, the actual value of k is sequenced through 1, 2, 4, et cetera until the value selected by the user is reached. The data is then further processed to prepare it for display. First, the fast processor performs any calculations required by the input selection. This may be as simple as **INPUT A** divided by **INPUT R** (A/R) or may be a very complicated user-defined expression. Next, the fast processor adjusts the phase of the data for the phase slope adjustment and then does the display function calculation (see Table I).

The two most common display functions (log magnitude and phase) have traditionally been implemented using a log amplifier and an analog phase detector. Because of the digital IF structure in the receiver (see Fig. 5), the HP 3577A's ability to do the detection digitally has greatly improved the stability and resolution of the analyzer's detector. The delay calculation is performed by approximating the derivative of phase ϕ with respect to frequency ω (Fig. 12). That is, group delay $= -\Delta\phi/\Delta\omega$, where $\Delta\omega =$ delay aperture.

Selectable delay apertures are provided (in percent of the selected frequency span) according to the number of data points used for the aperture. This allows the user to trade off noise reduction (provided by a wide aperture) and frequency resolution (provided by a narrow aperture) to optimize the group delay measurement. Apertures of 0.5, 1, 2, 4, 8, and 16 percent of the frequency span are provided and the resulting delay aperture is displayed in hertz. Previous analyzers provided only a fixed delay aperture, which could result in the aperture being wider than the bandwidth of the device under test. This difficulty is eliminated in the HP 3577A, because the delay aperture automatically tracks the selected frequency span.

Software

The software structure is shown in Fig. 13. EXECUTIVE, the highest-level module, performs the process scheduling function. EXECUTIVE maintains a table that indicates the status of each process and its priority. The highest-priority process that is ready to run will be executed. Processes can schedule other processes to be run as appropriate and processes can cancel other processes when they are no longer needed. This approach provides an orderly means of controlling the large software system. EXECUTIVE normally alternates between executing SWEEP CONTROL and COMMAND INTERPRETER.

Table I
Display Function Calculations

Function	Calculation
Log Magnitude	$10\log(R^2 + X^2)$
Linear Magnitude	$\sqrt{R^2 + X^2}$
Phase	$\tan^{-1}(X/R)$
Real	R
Imaginary	X
Polar	R versus X
Group Delay	$-\Delta\phi/\Delta\omega$

SWEEP CONTROL coordinates the synthesizer, the output board, and the fast processor in performing the sweep functions in the instrument. It also keeps track of when the digital marker information must be updated and does so when the sweep passes the marker location. At the start of each sweep, SWEEP CONTROL generates a list of instructions for the fast processor hardware to execute and sets up the control ports in the analog sections. During the sweep, SWEEP CONTROL keeps track of the activities of the fast processor and analog circuits by acting as a software state machine. Events in the fast processor cause SWEEP CONTROL to transition from one state to the next. This state machine approach keeps an extremely complex real-time task manageable. SWEEP MANAGER initializes the fast processor and the fractional-N frequency synthesizer and sets up the sweep.

COMMAND INTERPRETER accepts commands from the front panel and the HP-IB interface, categorizes each command and invokes the appropriate subordinate module. This is the largest process in the instrument software; it includes menu generation, user-defined math support, plotter control, HP-IB command parsing, numeric entry, RPG (rotary pulse generator or knob) entry, and general command execution. Corresponding HP-IB commands and front-panel key presses are translated into the same internal tokens by COMMAND INTERPRETER and passed on to the appropriate subordinate module for execution. This makes command processing for the HP-IB and the front panel consistent, minimizes duplicate code, and streamlines the software structure.

CONFIDENCE TEST and 1 PORT CALIBRATION are less-used processes that implement their respective features by emitting commands that COMMAND INTERPRETER executes.

A system of message queues allows communication between processes. One process may need to provide information to another process before it is executed so that the receiving process knows what action is required. The sending process puts the message in the message queue of the receiving process. When the receiving process is executed, it first looks in its queue to determine what messages are there and then determines what action is required.

Some sections of the software are so critical that they are interrupt driven. The MC68000 main microprocessor has seven levels of interrupt, five of which are used. The highest-level interrupt (level 7) is connected to the **INSTR**ument **PRESET** key on the front panel. Level 6 is used by the fast processor to transfer trace data to the main processor in real time. Level 5 is used by the fast processor to transfer status information. The status interrupt procedure performs only the critical tasks and then puts the status message in the SWEEP CONTROL message queue to be processed later. Level 4 is the system timer, a divided-down version of the 10-MHz reference that interrupts the main processor at a 6-Hz rate. This interrupt is used to scan the keyboard and update a software real-time clock. Interrupt level 3 is used in conjunction with the TMS9914A HP-IB interface circuit to implement the HP-IB functions.

The firmware for the main processor was developed using a Pascal workstation based on an HP 9000 Series 200 Computer. The richness of the Pascal dialect and the excellent computing power and memory size of the Series 200

were combined with some custom utilities to provide an efficient software development workstation. These workstations were then networked together with a shared resource manager (HP 9000 Model 226 Computer, Option 500) that allows access to a common disc and printer as well as a means of transferring data between workstations. Since both the Series 200 Computers and the HP 3577A Analyzer use an MC68000 microprocessor, the software developed on these workstations was inherently portable to the HP 3577A.

Approximately 90% of the instrument's firmware was written in Pascal and 10% was written in assembler code. There are approximately 40,000 lines of source code, which were compiled into 256K bytes of MC68000 machine code.

Servicing Features

The HP 3577A provides two means of assuring proper operation of its circuits. First, the instrument performs a variety of self-tests without the need for customer interaction. On power-up, the main processor RAM and ROM are tested, trace memory is tested, various system clocks are checked for activity, and the fast processor performs a self-test. The main processor also continuously monitors the status of the Analog Failure signal, which is an open-collector logic signal that is pulled low when a failure is sensed in the analog section. Second, a confidence test is included that requires the user to connect the source output to a receiver input with a short cable. The user can invoke this test to verify the functionality of the instrument. The analyzer does several frequency sweeps and checks the measured data against limits to determine whether a failure has occurred. Because of the high performance of the instrument, this is not a test to full specifications, but instead merely a test of whether the instrument is functional.

Acknowledgments

Many people contributed to the development of the HP 3577A Network Analyzer. During the definition phase of the instrument development, Howard Hilton, Greg Lipinski, and Chuck Platz contributed to the analog block diagram, digital hardware, and instrument control software. Other hardware contributors were Tom Fetter, Steve Venzke, Dave Potson, and Mike Maslaney. Dick Huffman provided much of the early mechanical design. Initial industrial design work was performed by Scott Lockhart and then Debbie Fromholzer.

The development phase of the project was completed by the following people. People contributing to the analog design areas are: Alan Baker, Joe Tarantino, Andy Cassino, Reid Adriance, Steve Bye, and Jay Kuhn. Mike Lamothe contributed both in digital hardware and software. Rick Pettit was instrumental in developing the custom digital filter integrated circuit as well as other digital hardware. The mechanical design of the HP 3577A was done by Bob Neel and Thatcher Harvey. The large software development task for the HP 3577A was accomplished by Dave Ringoen, Harry Plate, Praful Bhansali, Steve Peterson, Kirsten Carlson, and Brad Haeger.

The final industrial design was done by Randy Eilert. Jim Pietsch contributed production engineering assistance and helped define and conduct many of the state-of-the-art measurements necessary to produce this product. Sandy Marchant performed the difficult duty of ensuring that parts were on hand when needed and provided the expertise to transfer the product from the R&D lab into the production environment.

References

1. K. Hasebe, W.R. Mason, and T.J. Zamborelli, "A Fast, Compact High-Quality Digital Display for Instrumentation Applications," *Hewlett-Packard Journal*, Vol. 33, no. 1, January 1982.
2. D.D. Danielson and S.E. Froseth, "A Synthesized Signal Source with Function Generator Capabilities," *Hewlett-Packard Journal*, Vol. 30, no. 1, January 1979.

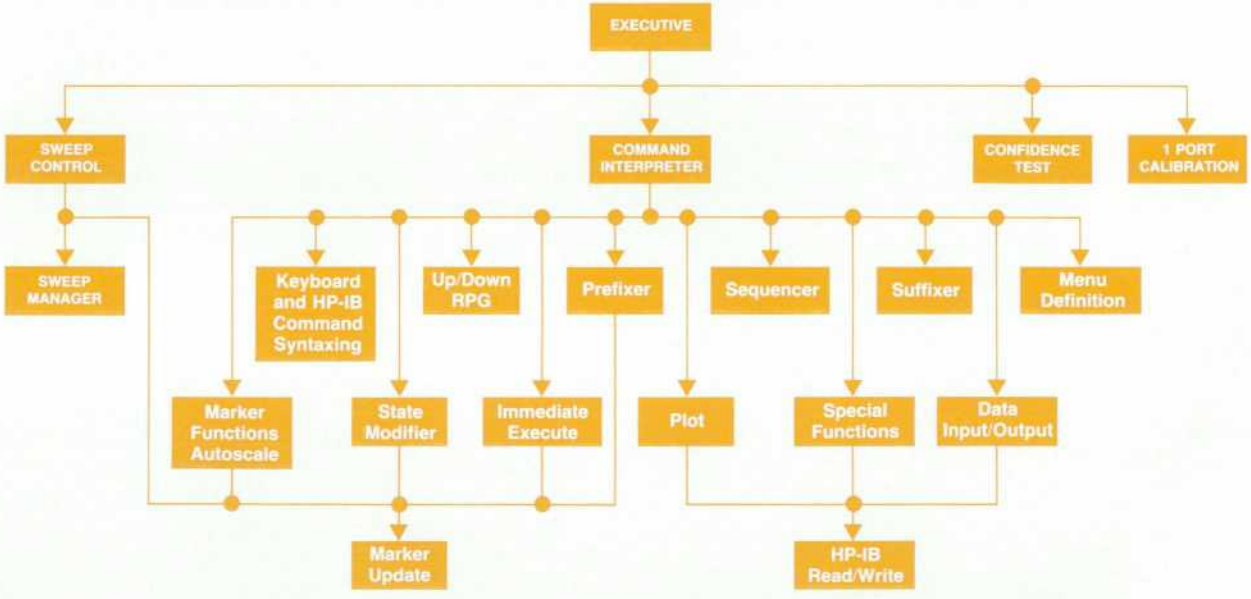


Fig. 13. *Operating system software hierarchy chart.*

A Broadband Two-Port S-Parameter Test Set

by William M. Spaulding

S-PARAMETERS allow network designers to characterize the transmission and reflection behavior of each port of a loaded N-port network in an accurate and easy-to-use manner. The scattering matrices formed by each network's S-parameters can be used to evaluate network matching under loaded conditions or can be easily combined to form one overall scattering matrix that characterizes a complex network formed of many smaller networks whose individual scattering matrices have been determined separately. To aid the designer in obtaining these useful parameters with the HP 3577A Network Analyzer (see article on page 4), a special test set was developed.

The HP 35677A/B S-Parameter Test Set (A for 50Ω systems, B for 75Ω systems) is based on the standard reflectometer bridge configuration that has been used in Hewlett-Packard instrumentation for many years (see Fig. 1). Early in the HP 35677A/B project, a decision was made to implement the test set as a "slave" unit by tapping the circuitry of the HP 3577A for power and control. A very simple, rear-panel, four-wire interconnect was developed as the complete interface. This approach provided the foundation for a very cost-effective instrument, and allowed the designers to focus on optimizing the RF design over a wide frequency range of 100 kHz to 200 MHz as the major development effort.

S-parameter measurements require the capability of distinguishing incident power from reflected power at the test ports. Two methods for separating incident and reflected waves are illustrated in Fig. 2 and Fig. 3. The schematic shown in Fig. 2a is representative of directional coupler circuits designed to function over a broad frequency range from LF (tens of kilohertz) to VHF and microwave. Individual circuit differences usually center on the manner in which the coupling transformers are implemented. At frequencies ranging from audio to low RF, transformers are often built using pot core or toroid designs. Mutual-imped-

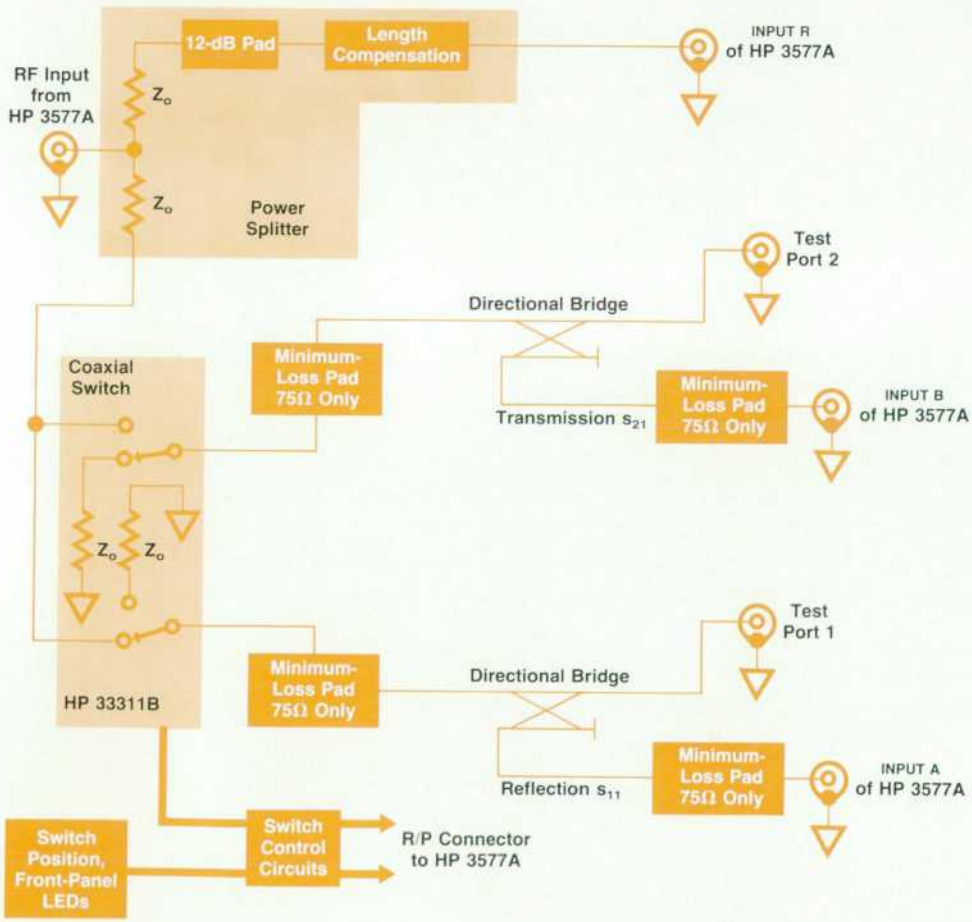


Fig. 1. *Block diagram of the HP 35677A/B S-Parameter Test Set. This test set is based on the standard reflectometer bridge configuration used by HP for many years, but required particular care in its design to cover a 100-kHz-to-200-MHz frequency range.*

ance-coupled lines are used as transformers as frequencies progress upward from RF to millimeter wavelengths. Fig. 2b shows an idealized circuit for the coupler which models transformer T1 as a scaled current source and transformer T2 as a scaled voltage source. Standard network analysis methods may be used to analyze the function of these circuits. From Fig. 2b it can be shown that:

$$V_{out} = (1/2N)[V_F + V_R - (I_F - I_R)R_{REF}] = (\Gamma/N)V_F$$

The voltage applied to the detector is proportional to the voltage reflection coefficient Γ scaled by the coupling factor 1/N. Common choices for the coupling factor are 1:10 or 1:100, yielding 20-dB and 40-dB couplers, respectively. A distinct advantage of the configuration of Fig. 2 is the ability to handle very large power levels, because of the 20-dB-to-40-dB loss to the detector port, while delivering full matched power from the source. The major disadvantage lies in the use of coupling transformers. At lower frequencies, coupling transformers can be realized to cover a frequency range on the order of a decade. Higher-frequency couplers are usually limited to octave frequency ranges because of bandwidth restrictions imposed by transformers implemented from coupled lines. Hence, multidecade bandwidths for these devices are not generally realizable.

Bridge Configuration

Fig. 3a shows the standard bridge configuration most often used to implement a multidecade reflectometer. As indicated by the circuit model of Fig. 3b, the function of the balun transformer is to float the single-ended voltage source across the bridge. In an alternative connection, the bridge could be driven single-ended from the source port and the balun used to float the detector (see Fig. 3c). The circuit shown in Fig. 3a was chosen for the HP 35677A/B, because the stray reactances of the balun are padded by the internal impedance of the bridge, resulting in a better detector port match. This can be an extremely important effect at the upper frequency limits of the system.

Although careful design is required, it is easier to implement the source balun in Fig. 3a than it is to implement the broadband transformers in Fig. 2a. By cascading two toroidal baluns wound from transmission line, a very high-performance balun covering a multidecade frequency range can be realized. At higher frequencies, the balun effect of a transmission line greater than one quarter wavelength in electrical length can be made to dominate as the transformer action of the toroids begins to fail. Higher-frequency test sets from Hewlett-Packard (e.g., the HP 8503A/B S-Parameter Test Set) use small semirigid coaxial line for the balun windings. The center conductor acts as the primary winding and the shield acts as the secondary winding.

Another alternative for the transmission line is to use wire carefully glued together at precise spacing to provide a parallel-wire line with the proper characteristic impedance. This line is then wound onto the toroidal cores using standard toroid winding machines to produce a bifilar-wound transformer. This approach is used in the HP 35677A/B. One balun is wound on very high-permeability, low-frequency, ferrite material to extend the frequency range downward. The second balun is wound on a more broadband ferrite material to provide transformer action at midrange frequencies. High-frequency performance is achieved by transmission-line balun effects as the line electrically becomes longer than one quarter wavelength. Over-

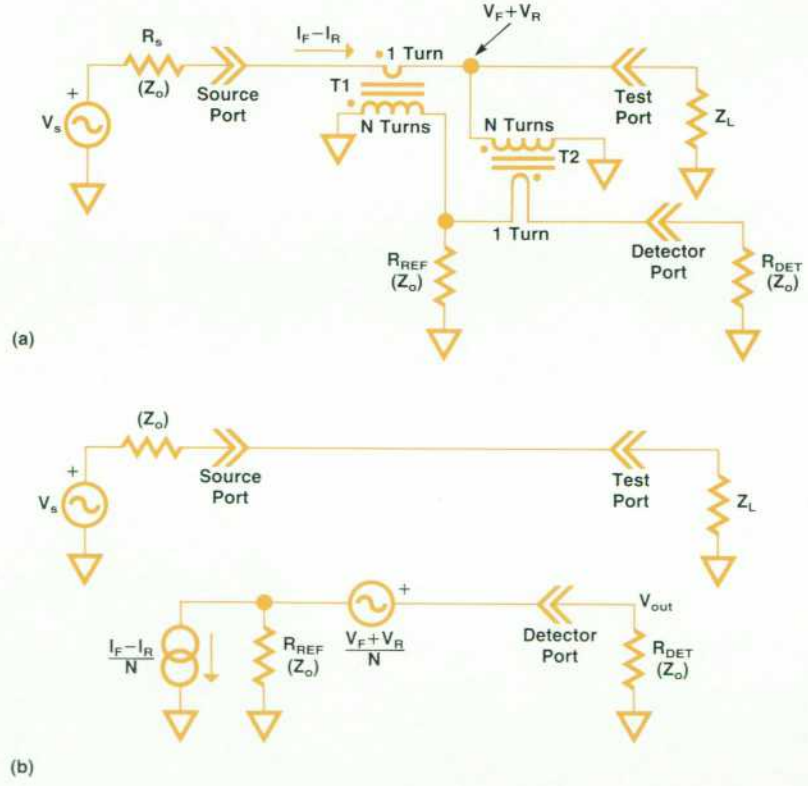


Fig. 2. *Directional coupler design for separating incident and reflected waves. (a) Circuit schematic. (b) Idealized circuit model. Z_o is either 50 ohms (HP 35677A) or 75 ohms (HP 35677B).*

all, extremely broadband performance results, covering a range in the HP 35677A/B that spans three decades and one octave (100 kHz to 200 MHz).

Stripline Design

Once baluns with satisfactory performance were designed, the engineering effort centered on the fabrication of the bridge circuit using standard G-10 epoxy-glass printed circuit techniques. One method used to achieve transmission lines on printed circuit boards is illustrated in Fig. 4. A trace of width w is etched on one side of the board with a ground plane covering the other side. The characteristic impedance of the stripline is determined using formulas such as those discussed in reference 1. Since the relative permittivity and dielectric losses of the printed circuit substrate material can vary significantly from batch to batch, the corresponding characteristic impedance and line insertion loss can also vary.

To preserve the cost advantage of using standard materials over having to use a substrate material with tightly controlled properties, the approach shown in Fig. 5 was chosen. In this approach, a machined housing functions as the ground plane and air is used as the dielectric. Since the plating is reasonably uniform over one side of the printed circuit substrate, the dimension d is controlled by the machining of the housing—a process that can be very accurate. No metal surfaces exist on the opposite side of the printed circuit board for distances many times greater than d. As a result, the per-unit-length capacitance of the line is determined primarily by the dielectric constant of air, with the effects of the properties of the printed circuit materials being almost totally negligible.

Directivity of the bridge corresponds to balancing its components on a one-to-one basis. Extreme care was taken to preserve symmetry in the printed circuit board artwork and to retain accuracy in the placement of the bridge components to maximize balance. A capacitance-adjustment screw was added to the reference resistor side of the circuit to allow for minor variations in capacitance at the test port.

Techniques similar to those described above were used in the design of the power splitter circuitry. Baluns and an attenuator pad were also placed in the reference path to equalize electrical length and insertion loss.

Acknowledgments

The author wishes to acknowledge the fine efforts of the

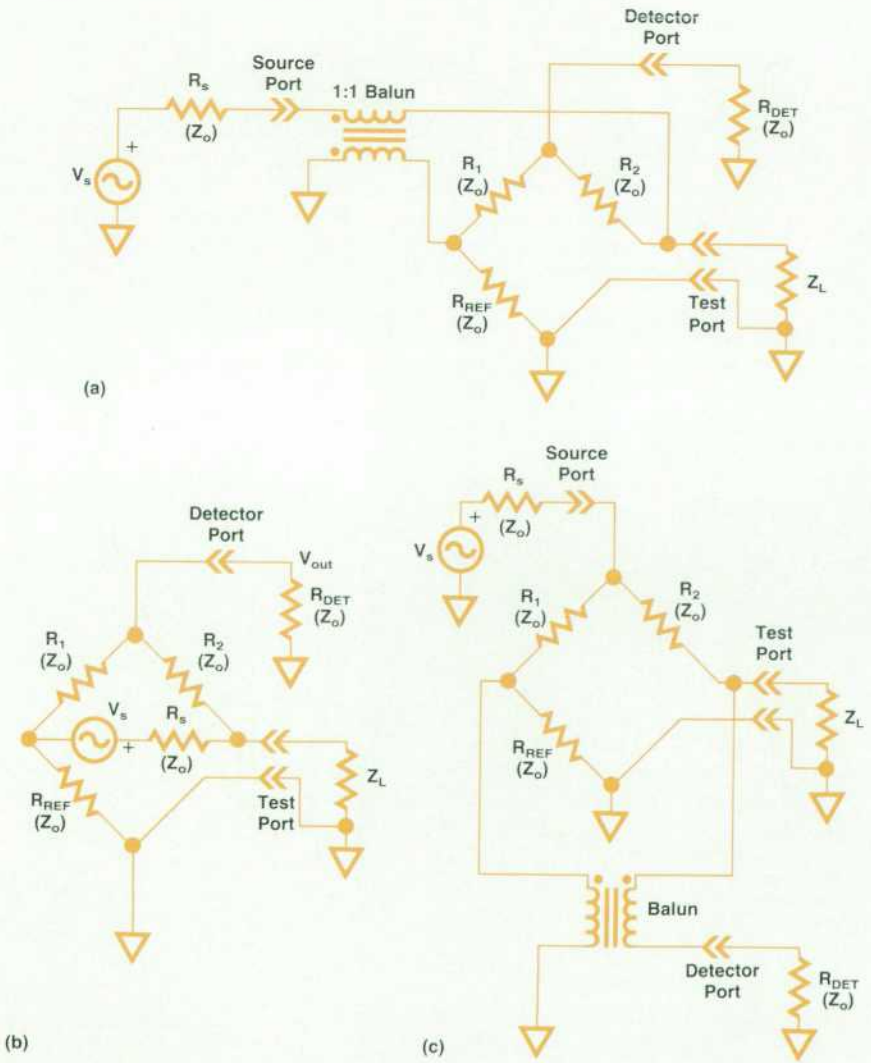


Fig. 3. *Directional bridge designs for separating incident and reflected waves. (a) Schematic of bridge circuit used in HP 35677A/B. (b) Idealized bridge model. (c) Alternative bridge circuit.*

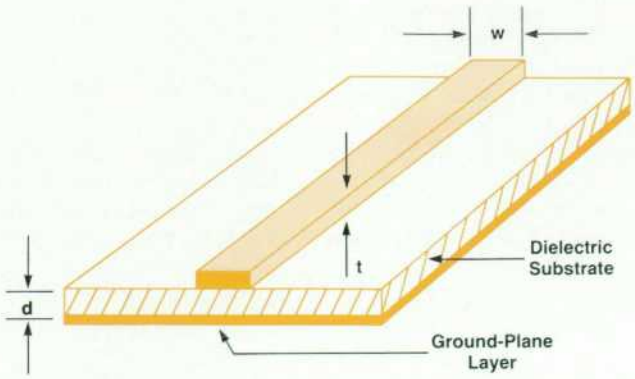


Fig. 4. *Standard strip transmission-line design for printed circuit boards.*

following people during the development of the HP 35677A/B Test Sets. Bill Ginder was the primary design engineer assigned to the project. His exceptional efforts in the areas of RF circuitry and bridge housing mechanical design helped to ensure a timely development cycle. Julius Botka of HP's Network Measurment Division was instrumental in bringing us up to speed in state-of-the-art bridge technologies. His advice and perspective were sincerely appreciated. Reid Adriance and Kirsten Carlson contributed to the control circuits and interface. Thatcher Harvey and Ann Testroet both provided design and packaging support with front-panel artwork and industrial design assistance from Debbie Fromholzer.

Reference

1. I.J. Bahl and D.K. Trivedi, "A Designer's Guide to Microstrip Line," *Microwaves*, May 1977, pp 174-182.

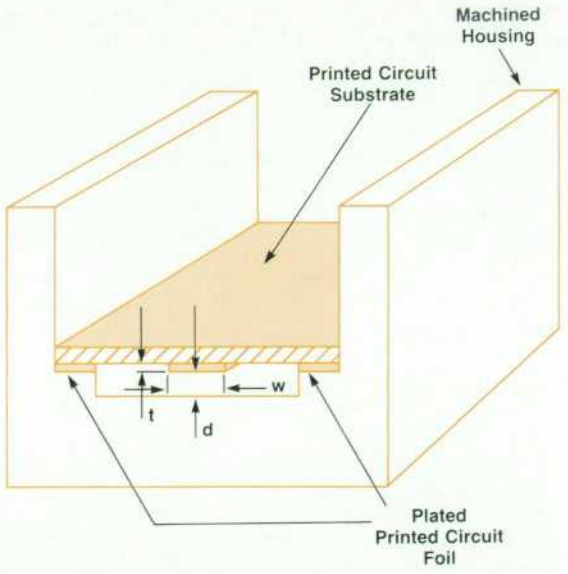


Fig. 5. *Strip transmission-line design used on the printed circuit boards in the HP 35677A/B S-Parameter Test Sets. This design minimizes the effects of variations in substrate material properties.*

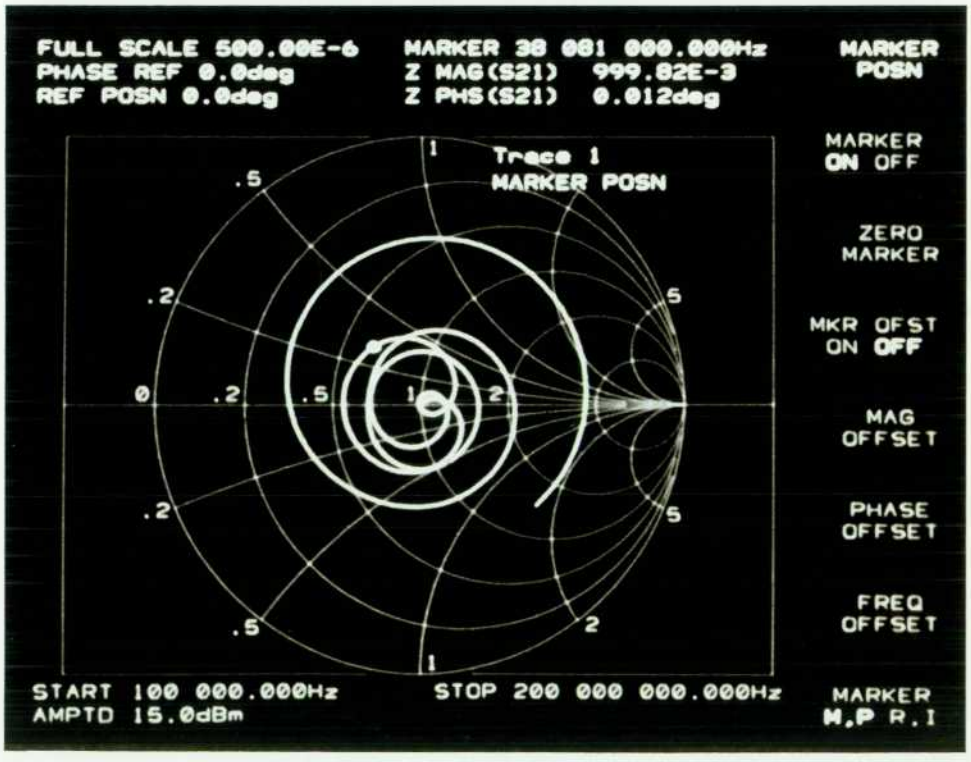


Fig. 6. *The broadband performance of the HP 35677A/B S-Parameter Test Sets combined with the features of the HP 3577A Network Analyzer allow measurement of an S-parameter, such as the transmission coefficient s_{21} shown here, over a range from 100 kHz to 200 MHz with one test setup.*

An ADC for a Network Analyzer Receiver

by Alan J. Baker

THE HIGH ACCURACY and resolution of the HP 3577A Network Analyzer are features that are made possible in part by the digital IF section and the analog-to-digital conversion scheme used in the receivers. Hence, resolution, linearity, and dynamic range of the HP 3577A are directly related to the performance of the analog-to-digital converter (ADC) used in its receivers.

The HP 3577A has an overall dynamic range of 100 dB, a dynamic accuracy (linearity) of ±0.02 dB over 40 dB of its dynamic range with some degradation over a wider dynamic range, and a resolution of 0.001 dB. The 100-dB dynamic range would seem to dictate that a 17-bit ADC be used in this application. However, full 17-bit linearity is not required at full scale, because the dynamic accuracy specification corresponds to only 9-bit linearity at that level. Furthermore, only a 15-bit linearity would be required to hold the dynamic accuracy specification for an input 40 dB below full scale (simply because six of the upper bits of the ADC are lost, that is, are zero at this input level). What is really required is an ADC that has enough linearity to meet the dynamic accuracy specification and that can be moved over the required dynamic range to reduce the maximum number of bits required.

As mentioned in the article on page 4, the HP 3577A receiver's ADC stage is constructed using a 12-bit successive-approximation A-to-D converter preceded by a prescaling amplifier. The gain of the amplifier is variable in 6-dB increments from 0 dB to 42 dB. When an A-to-D conversion begins, the gain is initially set to 0 dB and the ADC performs a quick eight-bit conversion to obtain an estimate of the input level. This eight-bit estimate is then used to address a ROM lookup table. The output of the lookup table is used to set the gain of the prescaling amplifier to the optimum value, that value being the gain that pushes the input to the ADC as near as possible to positive or negative full scale without exceeding full scale. Then, the ADC performs a more accurate 12-bit conversion.

This arrangement is essentially a floating-point analog-to-digital converter. The result of the 12-bit conversion represents the mantissa, and the gain setting for the prescaling amplifier represents the binary exponent. Fig. 1 is a simplified block diagram of the A-to-D conversion section of the HP 3577A's receivers. As shown in this diagram, the result of the 12-bit conversion is postmultiplied by the reciprocal of the gain of the prescaling amplifier or 1/G. This is analogous to multiplying by a binary exponent and is accomplished by appending the appropriate number of zeros to the 12-bit result from the ADC. This technique provides an ADC that runs at an 8-kHz conversion rate with 0.004-dB resolution, better than ±0.02-dB dynamic accuracy, and greater than 100-dB dynamic range. The resolution is improved to better than 0.001 dB by averaging multiple samples in the presence of noise.

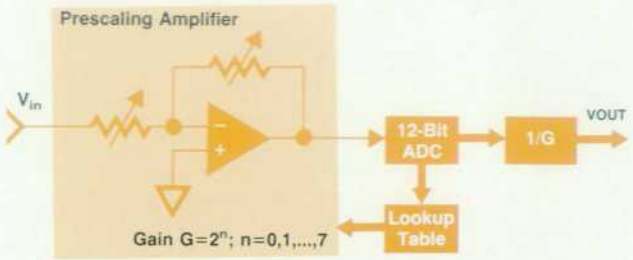


Fig. 1. *Simplified block diagram of the analog-to-digital conversion section used in the three receivers of the HP 3577A Network Analyzer.*

Fig. 2 gives a more detailed picture of the prescaling amplifier. This amplifier is a standard inverting amplifier and its gain is varied by changing the position of the summing node relative to the resistor network through the use of FET switches. Only one of the FETs is ever on at any given time. The series sum of the resistors to the left of the on FET corresponds to the amplifier's input resistor and the series sum of the resistors to the right of the on FET corresponds to its feedback resistor. The resistor network

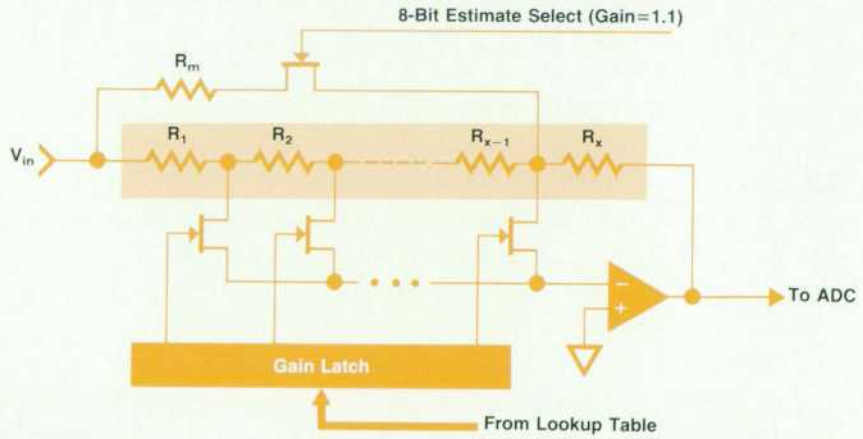


Fig. 2. *Prescaling amplifier used with the receiver ADC.*

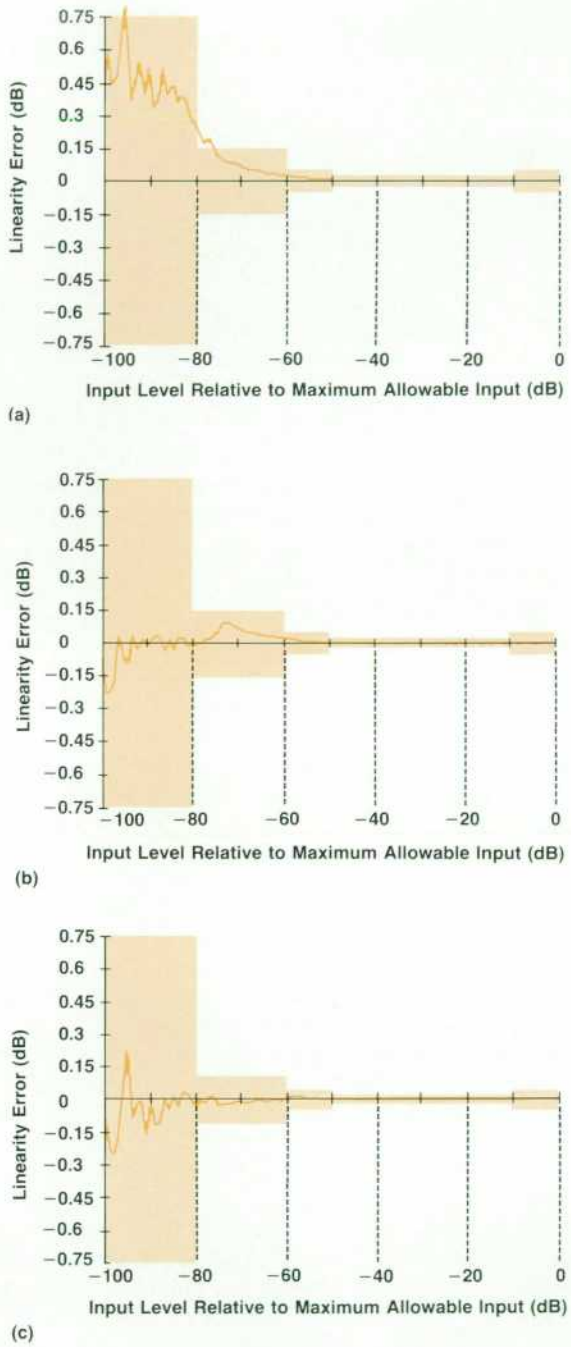


Fig. 3. *Effect on linearity error of offsetting the input signal a small amount. The shaded region defines the HP 3577A's linearity specification. (a) Linearity error caused by one LSB error in the MSB transition of the ADC. No signal offset. (b) Reduction of error in (a) by offsetting input signal by only 0.013% of full scale. (c) Further reduction of linearity error in (a) by offsetting input signal by 0.07% of full scale.*

is a patterned thin film of tantalum nitride. The thin-film resistors are ratio-trimmed to ±0.02% to provide the required A-to-D conversion linearity. Guarding techniques and low-leakage FETs are used in the prescaling amplifier circuit to prevent leakage currents from summing into the amplifier and introducing nonlinearities.

The resistor R_m in Fig. 2 is only switched into the circuit when the eight-bit estimate of the input is being made. Ideally, this estimate is made with the gain of the prescaling amplifier set to one (0 dB). To provide some margin in the eight-bit estimate, the gain of the amplifier is actually set to 1.1 instead of one by switching R_m in parallel with the effective input resistor. This 10% margin ensures that the input to the ADC does not exceed full scale when the optimum gain value is selected from the eight-bit estimate for the subsequent 12-bit conversion.

The 12-bit ADC is used in a bipolar mode. That is, the most-significant bit (MSB) of the 12-bit result is a sign bit so that the mantissa is represented in sign-inverted two's-complement form. The MSB transition occurs in the region of zero volts. Consequently, small input signals fall into the MSB transition region and an error in the MSB transition will create a dynamic linearity error at small signal levels. Since dynamic linearity is a ratio error (the ratio of the measurement error to the input signal level), the dynamic linearity can be improved by offsetting the input to the ADC slightly so that small inputs are biased out of the MSB transition region. Granted, there are code errors associated with other bits of the ADC output. However, if the input signal is offset by only a small amount so that it doesn't fall into the region of another major bit transition, the noise on the input smooths out the errors associated with the least-significant bits (LSBs). The digital filtering that follows the ADC effectively averages multiple A-to-D samples and provides this smoothing.

Fig. 3a shows the linearity error that results because of a one-LSB error in the MSB transition of the ADC. Fig. 3b shows the improved linearity when the input signal is offset by only 0.013% of full scale. Fig. 3c shows the further improvement in linearity for an offset of 0.07% of full scale. The input offset is adjusted at the factory to provide the required linearity.

Fig. 4 is a model of the A-to-D conversion section that includes the various offsets associated with this section of circuitry. These offsets can create several types of linearity errors if not adjusted properly. V_{os_0} is the offset associated with all of the circuitry before the A-to-D conversion section. This offset is adjustable. V_{os_1} is the offset associated with the prescaling amplifier and can also be adjusted. Finally, V_{os_2} is the input offset associated with the 12-bit ADC and is not adjusted in this scheme.

From Fig. 4, the expression that describes the digital output as a function of the analog input voltage is:

$$VOUT = [-G\,(V_{in} + V_{os_0}) + (G+1)\,V_{os_1} + V_{os_2}] \times 1/G \qquad (1)$$

which may be reduced to:

$$VOUT = -(V_{in} + V_{os_0} - V_{os_1}) + (V_{os_1} + V_{os_2})/G \qquad (2)$$

Note that V_{os_1} is referred back to the input. That is, V_{os_1} appears in the same term that contains V_{in} and V_{os_0}. This term is independent of the gain selected. The second term is an offset term that scales with the selected gain. Recall that to select the optimum gain, the prescaling amplifier is first set to a gain of 1.1 to obtain an eight-bit estimate of the input signal level. When a gain of 1.1 is selected, the second term of Equation 2 may be a significant percentage

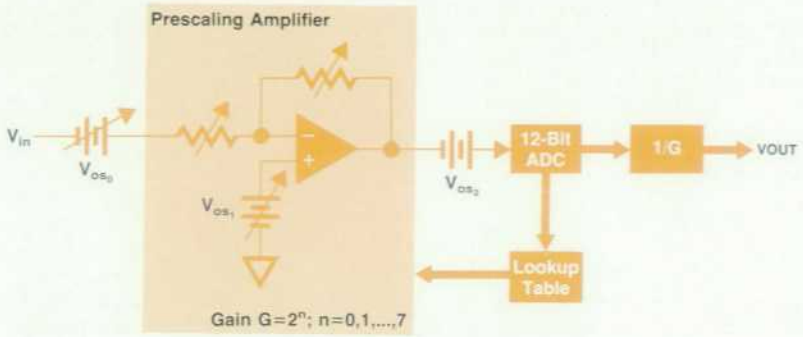


Fig. 4. *Simplified model from Fig. 1 with various offset voltages included.*

of the total answer if V_{os_1} and V_{os_2} are significant. Consequently, the estimated signal level can be in error by a significant amount, resulting in an improper gain selection for the 12-bit A-to-D conversion. In some cases, the incorrect gain chosen may cause the input to the ADC to exceed full scale, the result being a spike in the dynamic linearity plot (see Fig. 5).

When measuring one or the other of the quadrature components of the input (either real or imaginary), the HP 3577A averages two samples that are 180 degrees out of phase, with the sign of one of the samples inverted. This sign inversion and averaging are done in the digital down-conversion and filtering stages that follow the ADC. The expression describing this process is:

$$\text{Measurement} = \tfrac{1}{2}\,\text{VOUT}|_{V_{in}} - \tfrac{1}{2}\,\text{VOUT}|_{-V_{in}} \qquad (3)$$

The gains associated with the positive and negative samples may not be the same. If the gain associated with the positive sample is G_p and the gain associated with the negative sample is G_n, then by inserting Equation 2 for V_{in} and $-V_{in}$ in Equation 3 we obtain:

$$\text{Measurement} = -V_{in} + \tfrac{1}{2}(V_{os_1} + V_{os_2})\,[(1/G_p) - (1/G_n)] \qquad (4)$$

Note that V_{os_0} is eliminated and does not appear in this equation. V_{os_0} is the offset used to bias small signals out of the MSB transition region of the ADC. This dc term is converted to an out-of-band term in the digital down-conversion stage that follows the ADC and therefore does not affect the measurement. The second term of the equation represents a measurement nonlinearity that occurs when the positive and negative gains are not the same (this occurs when the input voltage is in the gain transition region).

Both of the problems just described (improper gain selection and a nonlinearity caused by different positive and negative gains) can be eliminated or reduced by adjusting V_{os_1} so that $V_{os_1} = -V_{os_2}$. When this is done, the error terms in Equations 2 and 4 go to zero. V_{os_1} is adjusted in the factory to eliminate these errors.

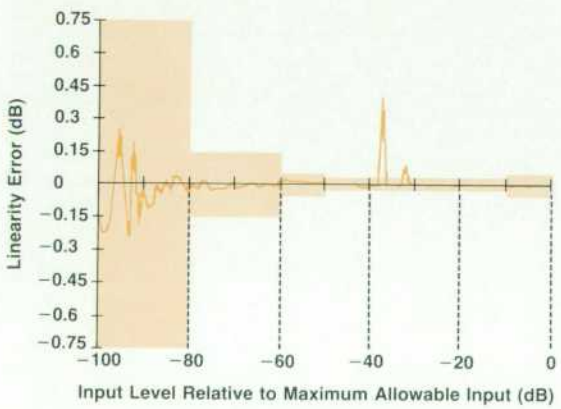


Fig. 5. *Effect of an error in the 12-bit A-to-D conversion gain selection on dynamic linearity (note spike near −40 dB input level). The shaded region defines the area of operation within specifications.*

Acknowledgments

The ADC architecture was originally conceived by Howard Hilton. Steve Venzke was responsible for much of the development of the ADC.

Authors

November 1984

4 — Network Analyzer

Jerry W. Daniels

Born in Fresno, California, Jerry Daniels studied electrical engineering at the University of California at Berkeley (BSEE 1967 and MSEE 1969). He then came to HP and has worked on a variety of HP instruments—the HP 3320 Synthesizer, the HP 3570 Network Analyzer, and the HP 3571 and HP 3585 Spectrum Analyzers. Jerry was a coauthor of an HP Journal article on the HP 3571 (May 1975) and is now project manager for the HP 3577A Network Analyzer. Living in Everett, Washington with his wife and two children, he spends his free time hiking, fishing, and sailing (both racing and cruising on Puget Sound).

Robert A. Witte

Currently teaching undergraduate electrical engineering courses at North Carolina Agricultural and Technical State University under the auspices of HP's faculty loan program, Bob Witte was the project manager for the digital hardware and software sections of the HP 3577A Analyzer. He started at HP in 1978 and holds a BSEE degree from Purdue University (1978) and an MSEE degree from Colorado State University (1981). He is a member of the IEEE, was born in Fort Wayne, Indiana, is married, and has a daughter. Although presently living in Greensboro, North Carolina, his home is at Lake Stevens, Washington. When not chatting with fellow amateur radio operators, he enjoys camping and hiking.

17 — S-Parameter Test Set

William M. Spaulding

Bill Spaulding is a design engineering project manager at HP's Lake Stevens Instrument Division. Besides his work on the HP 3577A Analyzer, he has made contributions to a number of HP instruments since joining the company in 1969. Most recently, his work has resulted in two patent applications related to signal synthesis. Born in Osceola, Iowa, Bill attended the University of Wyoming (BSEE 1967) and the University of New Mexico (MSEE 1969). He is married, has two daughters and a son, and lives in Everett, Washington. Outside of work, he is interested in model railroading, radio-controlled model airplanes, and amateur radio (NA7Y), where he often can be found working CW on 20 meters.

21 — Analyzer Receiver ADC

Alan J. Baker

Joining HP in 1978, Alan Baker initially worked on angle transducers for HP's surveying instruments. This work resulted in four patent applications. In 1982 he transferred to the Lake Stevens Division and was assigned responsibility for the receiver and reference sections of the HP 3577A Analyzer. Alan studied electrical engineering at Brigham Young University, earning a BS degree in 1978 and an MSE degree in 1980. Born in Seattle, Washington, he now lives in nearby Everett with his wife and two children. He is active in his church and enjoys hiking, camping, and skiing in the Pacific Northwest.

25 — Industrial Terminal

Jean-Claude Dureau

Jean-Claude Dureau is an R&D mechanical engineer at HP's Grenoble Personal Computer Division. His major contribution to the HP 3081A was the design of the technology used for sealing the case, the connectors, and the new keyboard system. Before joining HP in 1980 he was employed in aerospace and physics research laboratories. He studied precision mechanics at the University of Besançon, and holds a DPE diploma in automatic control and robotics from the University of Paris. After working some years in the Federal Republic of Germany and the U.S.A., he now lives with his wife and two daughters in Grenoble. He enjoys skiing and is very fond of sailing.

Jacques Firdmann

Jacques Firdmann is an industrial designer with HP's Grenoble Division. He did the industrial design of the HP 3081A Terminal. With HP since 1977, he has also designed enhancements for the HP 307X and HP 262X families of terminals. Before joining HP, he designed products for a manufacturer of toilet accessories and plastic furniture. Jacques is a graduate of the Ecole Nationale Supérieure des Arts et Metiers. He is married, has three children, and lives in Grenoble. He's a student of karate and plays volleyball and tennis.

Jean Bounaix

Jean Bounaix grew up in Paris, France and studied electronic engineering at the Institut Polytechnique of Grenoble. Before joining HP's Grenoble Division in 1977, he worked as a designer of minicomputer hardware. Jean was project manager for the HP 3081A and is now involved in telephone and voice personal computer products. Living in Grenoble, he enjoys skiing and sailing, and as an avid private pilot, actively participates in the young HP Grenoble flying club.

30 — Printer Family

Mark J. DiVittorio

Born in Chicago, Illinois, Mark DiVittorio came west to study electrical engineering and computer science at the University of Santa Clara (EECS 1974 and MSCS 1980). He started work at HP in 1975 as a production engineer for the HP 264X Terminals, later moved to R&D to work on the HP 2647 Terminal, and then joined the Vancouver Division where he is now project manager for the HP 2933A and HP 2934A Printers. Mark is married, has one son, and lives in Vancouver, Washington. His interests include programming, fly tying, salmon and steelhead fishing, and radio-controlled boats and tanks (the latter occasionally destroying the plants in his yard).

33 — Printer Control IC

Thomas B. Pritchard

Tom Pritchard joined HP in 1978 after receiving a BSEE degree from the University of Cincinnati. He began as a production engineer for the HP 3000 Series 33 Computer and later transferred to the Vancouver Division to do R&D on a variety of HP printer products, including a thermal print mechanism, the processor board and firmware for the HP 2671 Printer, and most recently, the firmware for the HP 2932 Printer and the custom IC described in his article. Outside of work, Tom is completing his studies for an MSEE degree at the University of Portland and tutors high school students in basic electronics and state machines. Born in Ann Arbor, Michigan, he is married and now lives in Vancouver, Washington. When not busy with environmental activities, he enjoys hiking, traveling, bicycle touring, and learning to play the recorder.

David S. Lee

Currently a development engineer for bar code products, Dave Lee worked on the custom IC for the HP 293X Printers. With HP since 1979, he has a BSEE degree awarded in 1977 by the University of Wyoming and an MSEE degree awarded in 1978 by Purdue University. Born in Shanghai, China, he now lives in San Jose, California and enjoys competition in tennis, bowling, soccer, table tennis, and foosball.

An Industrial Workstation Terminal for Harsh Environments

This terminal is designed to collect production data right at the source on the shop floor in adverse environmental conditions.

by Jean Bounaix, Jean-Claude Dureau, and Jacques Firdmann

IN THE INDUSTRIAL WORLD TODAY, competition is strong and is focused on price and quality. Production management has to keep a close watch on materials, labor, processes, and goods. To help production people in their decision processes, application programs can provide real-time data synthesis, but their results are meaningful only if the data has been picked up right at the source—the production line.

HP's new industrial workstation terminal, the HP 3081A (Fig. 1), is designed to meet this need. It can go into hostile environments characterized by dust, humidity, liquid jets, chemical pollution, repetitive vibrations or shocks, and strong electromagnetic disturbances. Its excellent resistance to the environment, especially to dust and liquids, makes it suitable for most industrial applications. The only limitations are temperatures below 0°C, or explosive atmospheres (the terminal is not gas-tight).

The HP 3081A Industrial Workstation Terminal is a compact, low-cost personal terminal. Its robust plastic casing ensures maximum rigidity and sturdiness as well as excellent resistance to a wide range of chemicals. Gasket seals along the casing halves and cable feedthroughs guarantee protection from dust and liquid penetration to an IP rating of 65, as defined in IEC Publication 529 (see page 26). The HP 3081A is tested as specified in this standard to verify its IP rating.

The terminal provides the untrained operator with very simple data input and output devices:

- One-line alphanumeric display. Messages up to 32 characters in length can guide operators step by step through their data collection transactions.
- Keyboard with large keys. Operators can use the keyboard to enter answers through user-definable function keys.
- Bar code reader. To shorten the data capture process when long alphanumeric data is entered, the keyboard can be bypassed by bar code input, which also significantly improves data integrity.

Fig. 1. *The HP 3081A Industrial Workstation Terminal is sealed against dust and liquids to an IP rating of 65. The standard numeric keypad has large keys that are easy to operate with gloves on.*

Fig. 2. *Options include an alphanumeric keypad, a choice of bar code wands, and a choice of slot readers.*

In its standard configuration, the HP 3081A is supplied with a numeric keypad with five function keys (10 with shift key), a 32-character alphanumeric display, and 2400-baud, current-loop data communications capability.

The display uses vacuum fluorescent technology, and has bright green 6×3-mm (0.24×0.12-in) characters.

For applications requiring alphabetic keyboard input, an optional full alphanumeric keyboard is available (Fig. 2). The ABCD sequential layout of the alphanumeric keyboard makes more sense to industrial users who are not familiar with typewriter or computer terminals and prefer to "hunt and peck" in alphabetical order.

The optional bar code reader is designed to provide more efficient data entry by greatly reducing the time and errors associated with keyboard entry. The amount of reduction varies, depending on what reports one reads or what assumptions one makes, but it is not unreasonable to expect that typically, entry time can be reduced by a factor of 10 over typing, while accuracy can be increased by a factor

of 1000. The terminal can be fitted with one of a range of six bar code readers, including handheld wands and slot readers for badges and edge-coded documents. A mounting bracket is available so that the terminal, as well as the wand or slot reader, can be secured to a wall or other flat surface.

Installation

The HP 3081A can be connected to a computer in a number of configurations. When used with an HP 92922A Four-Channel Adapter or an HP 92923A Single-Channel Adapter (point-to-point) or with an HP 2333A Cluster Controller (multipoint), the HP 3081A is powered by a dc voltage (12V to 36V) routed through the datacom cable from the adapter or the controller. When the HP 3081A is used as a stand-alone (OEM) terminal, an external dc power supply is required.

The HP 3081A can be connected to an RS-232-C point-to-point port on almost any computer through the HP 92922A Adapter (up to four terminals per adapter) or the HP 92923A Adapter (one terminal per adapter). It can also be a component in a distributed network of terminals connected through the HP 2333A Cluster Controller (up to 32 terminals per controller). Fig. 3 and Fig. 4 illustrate these two connection methods.

A screwdriver is all that is needed to connect the current-loop datacom cable (no soldering necessary). The choice of current-loop cable, which is available in two versions (standard and special), depends on the datacom distance. The cable is screw-connected inside the rear access panel of the terminal. A gasket along the panel edge maintains the terminal seal. The optional bar code reader (wand or slot reader), is also screw-connected inside the same panel.

Datacom Distance

For end-user applications, HP provides two datacom cables, which allow a maximum of 60 meters (HP 92920A) or 150 meters (HP 92921A) between the HP 3081A and the

How Do You Describe Terminal Ruggedness?

The HP 3081A Industrial Workstation Terminal has an IP rating of 65. The industrial bar code wands have an IP rating of 64 while the bar code slot reader is rated IP 65. What does this mean?

These ratings are based on a standard (Publication 529-1978) provided by the International Electrotechnical Commission (IEC), which is affiliated with the International Organization for Standardization (ISO). The standard classifies degrees of protection provided by the enclosures of electrical equipment. After the letters "IP" you see a pair of numerals. The first number represents the degree of protection against particles, and the second represents the degree of protection against liquids. The accompanying table describes the degrees of protection.

IEC Standard for Classifying Enclosures

Class	Particles	Liquids
0	No protection	No protection
1	>50 mm (e.g., hand)	Protected from dripping water (vertical only)
2	>12 mm (e.g., finger)	Protected from dripping water (±15 degrees from vertical)
3	>2.5 mm (e.g., screwdriver)	Protected from splashing water (±60 degrees from vertical)
4	>1 mm (e.g., steel wire)	Protected from splashing water (any direction)
5	>75 μm (e.g., metal filings)*	Protected from water jets (0.3 bar, 12.5 liter/min)
6	Total protection from dust whatever the particle size	Protected from water jets (1 bar, 100 liter/min)
7		Protected from accidental immersion (150 mm depth)
8		Protected from continuous immersion

*Smaller particles cannot penetrate the enclosure in amounts sufficient to disrupt operation.

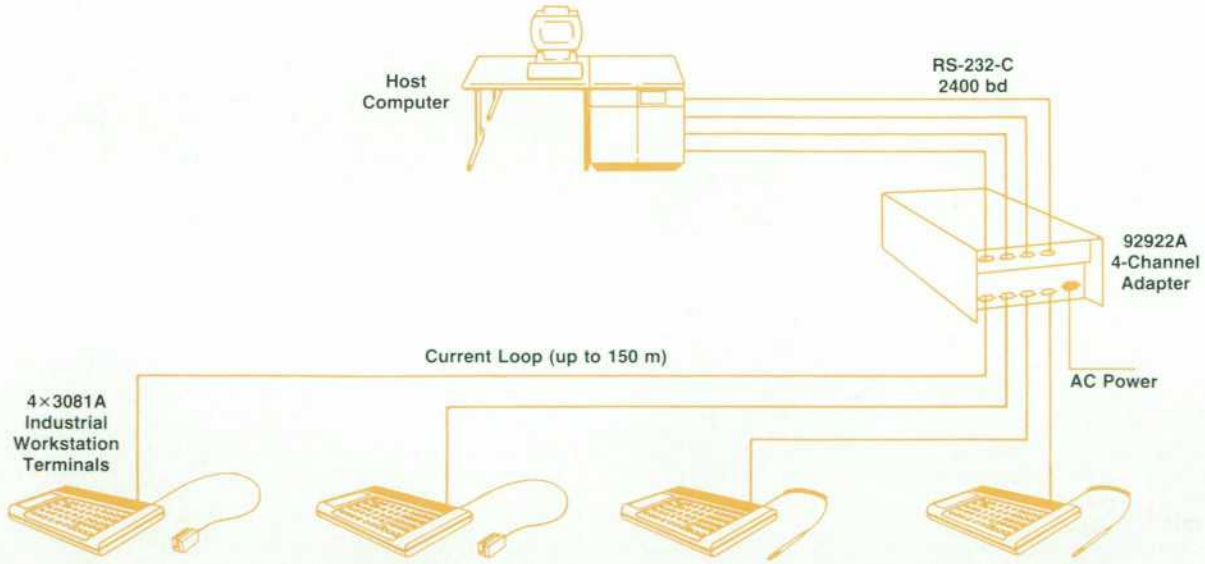


Fig. 3. *Point-to-point connections of the HP 3081A to an RS-232-C computer can use the HP 92922A Four-Channel Adapter or the HP 92923A Single-Channel Adapter (not shown).*

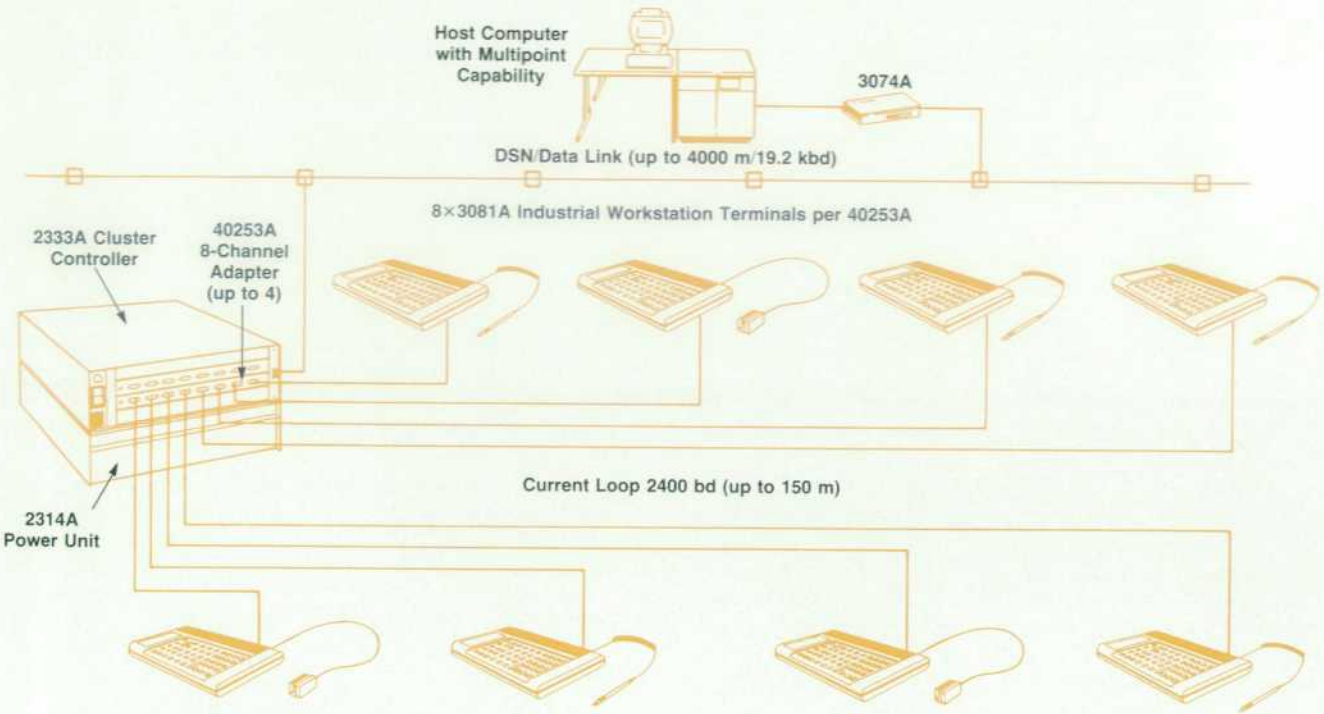


Fig. 4. *Multipoint short-distance connections of HP 3081As to a host computer can use the HP 2333A Cluster Controller with HP 40253A Eight-Channel Adapters.*

HP 92922A, HP 92923A, or HP 2333A.

For hardware OEMs who want to use their own cables, it is possible to extend this length, provided that a cable with lower electrical resistance is used. Two major precautions are necessary. First, the input voltage at the terminal must not be lower than 12 volts dc, and the voltage drop in the ground wire must not exceed 2.5 volts. The voltage drop in the ground wire represents a common-mode voltage, since the same ground wire is used for datacom and power. A separate ground wire for the power supply can be used to avoid this problem. Second, the external diameter of the cable must be between 3.5 and 6.5 mm to maintain the terminal seal.

If an OEM wants to configure the HP 3081A with a local power supply (i.e., if neither the HP 92922A/23A nor the HP 2333A is used), the distance is restricted by current-loop datacom requirements (600 meters or 1960 feet), rather than by cable resistance.

Note that HP does not provide or support low-resistance cable or a local power supply.

Design

The electronic circuitry is designed to implement the terminal functions at the lowest possible cost compatible with moderate volume. Standard but functionally efficient components were chosen. A single printed circuit board based on one microcomputer chip carries about one hundred components, as shown in Fig. 5. (CRT terminals today typically have more than four hundred). While the electronics of the terminal have been significantly simplified, the major design points are the sealed case, keyboard, and connection panel.

Case

Three criteria influenced the design of the case. First, the internal electronics had to be protected from the harsh industrial environment. Second, the electronic connections also had to be protected. And third, the cost had to be low. A sealed case, dust- and liquid-resistant, offers a solution to the problem of protecting the internal electronics. Waterproof connections often found in specialized military and industrial applications were available and could have solved the second problem, but their cost and complexity eliminated this choice. Instead, the connec-

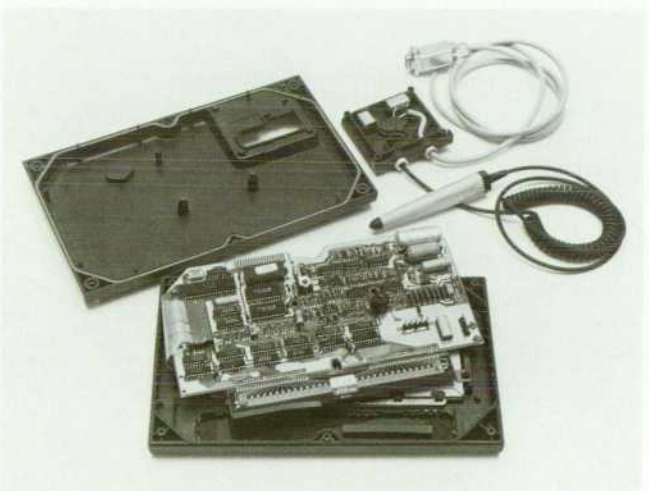


Fig. 5. *The HP 3081A's simplified electronics are on a single printed circuit board.*

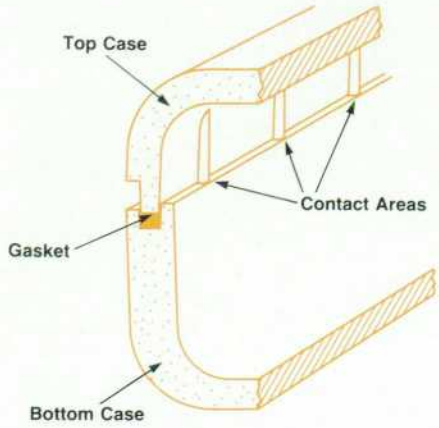


Fig. 6. *The case is sealed by toroidal gaskets pressed into grooves.*

tions are placed inside the case.

The case is made of ABS plastic, grade KJB. This material has good mechanical properties, shock resistance (stretching under temperature), and good chemical resistance to acids, bases, solvents, and oils. The sealing function is implemented differently for the case, the keyboard, and the connections.

For sealing of the case, toroidal gaskets are pressed into constant-volume grooves (Fig. 6). This technology is used to seal the assembly of the top and bottom halves of the case, the display window on the top of the case, and the connector panel in the case bottom. For sealing of the keyboard, hard lips are pressed on a flat gasket made by the elastomer keyboard itself (Fig. 7). This technology was chosen since it allows some give in the keyboard. A constant retaining force is provided by six steel springs.

The two electrical connections, one for the combined power supply and data communications cable and the other for the bar code reader cable, are protected under a panel connector, which is sealed with a toroidal gasket. These two openings are sealed with well known feedthrough conduit used in military and industrial applications (Fig. 8).

Display

For reasons of ergonomics, we decided to use a display that provides good visibility in both dim and brightly lit environments. The green display characters are more easily perceived by the human eye. A tilt angle of 10 degrees offers ease in reading whether the terminal is wall-mounted or placed on a table.

For cost and reliability reasons, we chose a direct connection with the printed circuit board (Fig. 9). A special curved pin was designed to give good flexion and protection from strains on solder points, on the glass, and on the board, both during assembly and later in use. Special tooling was developed to curve and locate 40 pins at the same time. Repetitive shock and vibration tests of long duration have demonstrated the quality of the connection system.

Keyboard

The sealed keyboard is a full-travel keyboard (1-mm travel) with tactile feedback. It is composed of (see Fig. 10):

- An elastomer keyboard for all mechanical keyboard functions, with the periphery functioning as a gasket that seals the top case
- A switch membrane circuit for electrical functions, with the following characteristics: switch contact of the keys,

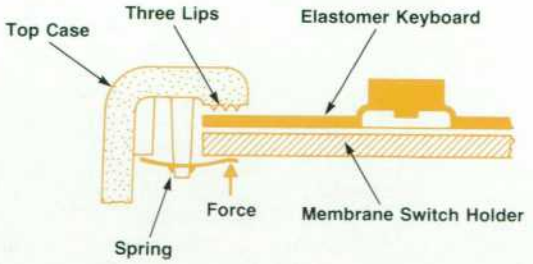
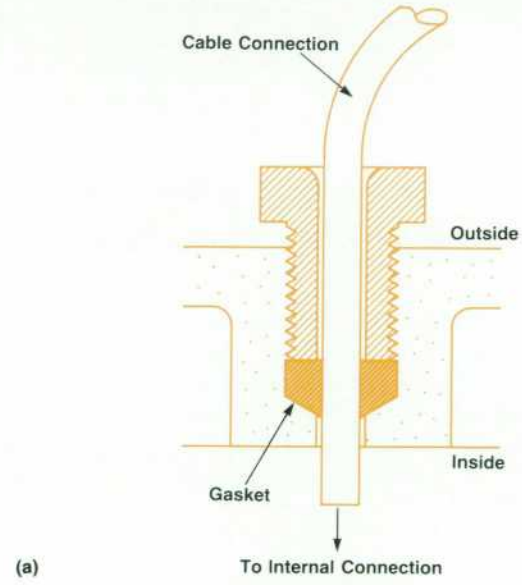


Fig. 7. *The keyboard is sealed by hard lips pressed into a flat gasket formed by the keyboard itself.*



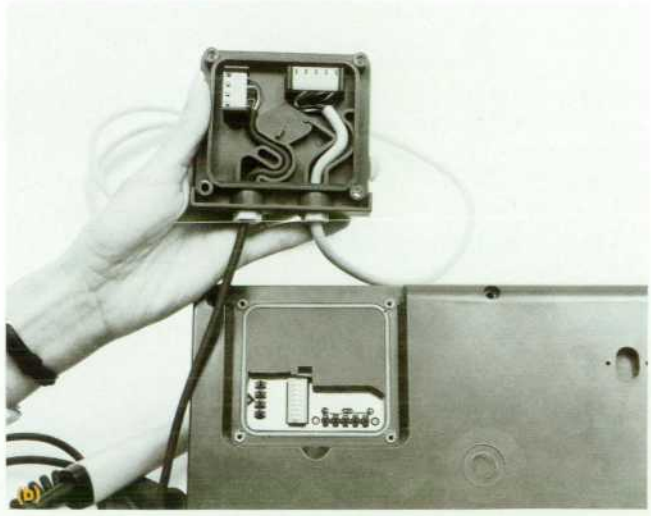


Fig. 8. *Cable connections are sealed with feedthrough conduits (a) and protected under a panel connector sealed with a toroidal gasket (b).*

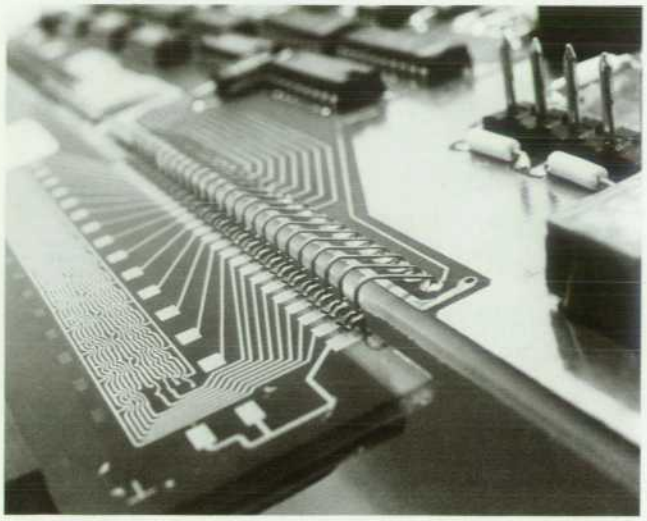


Fig. 9. *The display is connected directly to the printed circuit board by means of specially curved pins.*

Fig. 10. *The keyboard assembly consists of an elastomer keyboard that also functions as a gasket to seal the top case, a switch membrane circuit, a holder plate, and an overlay.*

sealing of the contact for double protection, connection circuit between the keyboard and the electronics board, and high dielectric isolation for protection from electrical discharges

- A holder plate for mechanical rigidity and mounting of the keyboard components
- An overlay for identification of the keys, definition of the keyboard workspace, and protection of the flexion area of the elastomer membrane underneath.

Industrial Design for Friendly Use

Although our primary objective was the construction of a rugged terminal, we wanted to achieve user acceptance in the factory environment by giving users a friendly terminal. The texture and color of the molded plastic case resist scratches and dirt. The keyboard has zones of different colors to facilitate the identification of keys. The shape and dimensions of the keys permit the use of gloves. The luminous display is easy to read in light or dark environments. A tough transparent cover allows the user to label the function keys. This cover slides to one side for label insertion or removal, but remains attached to the terminal so that it cannot be lost.

Although it is aimed at industrial use, the terminal is not out of place in the office or reception room.

Acknowledgments

There were several engineers who made significant contributions to the development of the terminal and the interfaces that support it. Roland Arthaud designed the terminal firmware and Jean-Pierre Dinet designed the terminal electronics. The interfaces in the HP 2333A Cluster Controller were designed by Jean-Marc Bonora and Joel Setton, while Bruno Souesme designed the subsystem power supply and the HP 92923A Single-Channel Adapter. The HP 92922A Four-Channel Adapter was designed by Jean Vandel, Alain Gateau, and Hugues de Charentenay. Claude Carpentier spent a long time on the mechanical tooling. Jean-Marc Laugenie made extensive system compatibility tests, helped by several HP 3000 and HP 1000 Division people. Jean-Francois Porret's safety and RFI gurus greatly helped us learn to live under the yoke of the FCC and VDE. Special thanks to Catherine Sottil and Dominique Dubus, who pushed all these products into production, and the rest of the fab personnel who made major efforts to help make the project a success.

High-Quality, Dot-Matrix Impact Printer Family

Easy paper handling, last-form tearoff, graphics, and a friendly control panel are some of the common features.

by Mark J. DiVittorio

HARD-COPY OUTPUT of results, reports, memos, order forms, charts, and program listings is frequently required for many computer applications. Equipment providing this output should be reliable, fast, and easy to use. Adding the requirement of high print quality, Hewlett-Packard developed the HP 293X Printer family to meet these needs.

The HP 2932A (Fig. 1), HP 2933A, and HP 2934A (Fig. 2) Printers are 136-column, bidirectional, dot-matrix impact printers. Common to the family is the ability to print at 200 characters per second (cps) on one-to-six-part forms up to 400 mm (15.75 inches) wide. The standard symbol font is designed to a 9×12 symbol cell matrix, with a horizontal and vertical resolution of 90 dots per inch (dpi). All three of the printers have the ability to print graphics at 21,600 dots per second. There are two standard character styles resident in all the printers—Courier (serif) and Cubic (sans serif). In addition, there are three standard pitches and ten resident languages, all of which can be selected from the printer's front panel or under host computer control.

One of the major features of this family is its simple and flexible paper handling. Various paper widths, labels, and multipart forms are accommodated. The adjustable feed tractors and the straight paper path ensure smooth movement of paper through the machine. The last-form tearoff capability (Fig. 1) saves paper, and front forms loading simplifies the task of loading and removing paper.

The interfaces offered include RS-232-C/V.24 (standard), HP-IB (IEEE 488), Centronics, RS-422, Data Link, and Synchronous Multipoint.

Architecture

There is a basic underlying architecture to serial dot-matrix printers (Fig. 3). The data is presented at an input/output port (HP-IB, RS-232-C/V.24, ...), processed electronically, converted to mechanical drive signals, and printed as characters on a piece of paper. The HP 293X Printers contain a microprocessor, RAM, ROM, a custom IC, and the power electronics for the printhead and motors; all of

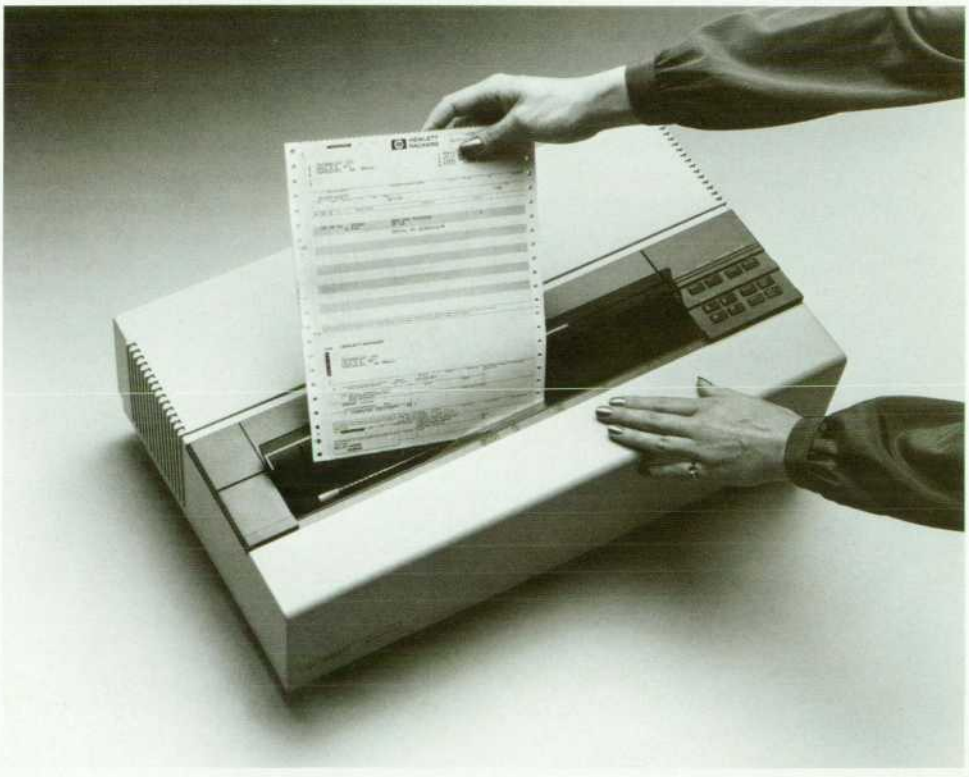


Fig. 1. *The HP 2932A General-Purpose Printer is the basic model of HP's 293X Printer family. All models feature last-form tearoff (shown), easy paper handling, graphics output, 200 character-per-second dot-matrix printing, and uncomplicated feature selection via a friendly front panel.*

this is required to convert the incoming data into the dots on the paper. In processing a simple character to be printed, the following must occur. The character is input, the character pattern in the character ROM is determined, and the code defining the dots that represent the character is fetched. The code for the dots is stored in a manner such that the twelve-wire printhead can be used efficiently. The custom IC handles a large portion of the details controlling the timing of when and how wires in the printhead are actuated to form the character.

Three of the major components of the HP 293X Printers are the impact printhead, the paper handling mechanism and the standard cell integrated circuit. This custom integrated circuit is discussed in the article on page 33. The printers also contain five printed circuit assemblies. The power supply electronics, the head and motor drivers, the I/O electronics, and the main logic electronics assemblies are interconnected through the fifth assembly, which functions as a main bus backplane.

HP 2932A and HP 2933A Printers

The HP 2932A General-Purpose Printer (Fig. 1) is the basic model of the HP 293X family. The HP 2933A Factory Data Printer has two additional features that were developed for use on the factory floor. This model will automatically generate bar code patterns and print large characters up to 28 times their normal size.

HP 2934A Printer

The HP 2934A Office Printer (Fig. 2) is the model that takes full advantage of the resolution of the mechanism and printhead that were designed for this printer family. The twelve-wire impact printhead, the paper handling mechanism, and the standard cell integrated circuit allow the HP 2934A to print near letter-quality (NLQ) text at 67 and 40 cps. The print quality is achieved by printing characters in a 36×24-dot character cell. At 67 cps the resolution is 90 dpi horizontally and 180 dpi vertically. At 40 cps the vertical resolution is identical to the horizontal resolution, 180 dpi. The 36-column-by-24-row NLQ cell is achieved with the twelve-wire printhead by printing the dots in the cell in two passes (Fig. 4). The twelve odd-numbered rows are printed, the paper is advanced a half dot width (0.0055 inch) and then the pattern for the even-numbered rows is overlaid on the first pattern.

The HP 2934A produces the near letter-quality characters by means of user-installable character cartridges. Four of these character cartridges may be resident in the machine at a time with each containing the data for a specific font at both printing speeds (67 cps and 40 cps). Fonts that are offered include Courier, Courier 12, Italic 10, Italic 12, and Letter Gothic. See Fig. 5 for some examples of the fonts printed by the HP 2934A.

NLQ Cells

The grid that the NLQ font symbols are designed within has 36 horizontal positions and 24 vertical positions (see Fig. 4). The purpose of the dense symbol cell is to allow better symbol definition and to simulate arcs with more precision. Not all of the positions can be used in a given symbol cell because, first, the impact frequency of a wire in the printhead is limited to 1800 Hz. Second, a line of text (when printed in the NLQ fonts) is printed with the printhead carriage moving at 20 inches per second. This rate, in conjunction with the impact frequency limit, limits the positions that can be printed in the 36×24 cell. The

Fig. 2. *The HP 2934A Office Printer offers letter-quality printing at 67 and 40 cps and memo-quality printing at 200 cps. High-quality graphics allows a user to add illustrations and graphs to reports and other documents printed on the HP 2934A. It is shown here with the HP 29340S Single Bin Sheet Feeder, an optional accessory for convenient use of company stationery and other single sheet forms.*

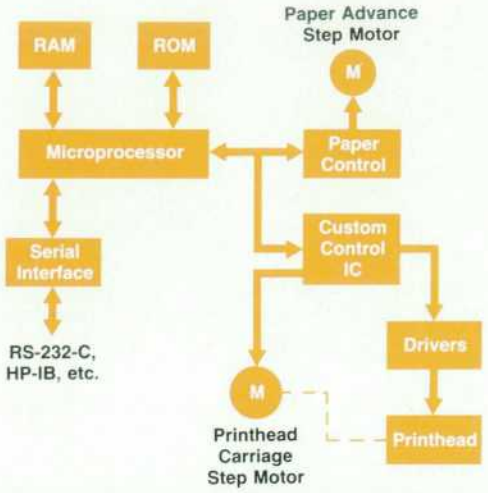


Fig. 3. *Basic block diagram of a serial dot-matrix printer.*

resulting limitation on a given wire is that it once it has been energized it cannot be energized again for four logical dot positions. However, this does not limit the logical cell pattern for a symbol to every fourth position in the horizontal direction. If a wire in a given row is fired in column zero, the next time it can be energized is column four. But,

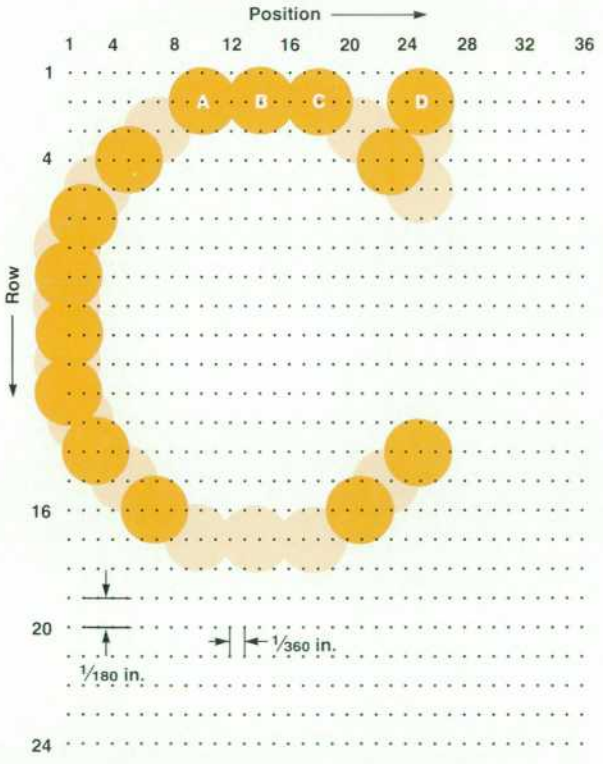


Fig. 4. *Near letter-quality character cells on the HP 2934A Printer are formed by two passes of the twelve-wire printhead as shown for the Courier letter C. Shaded dots are formed on the first pass, solid dots on the second pass. Because of printwire impact frequency and printhead carriage velocity limitations, dot spacing in any row of an NLQ cell cannot be any closer than one dot every four horizontal dot locations (see text).*

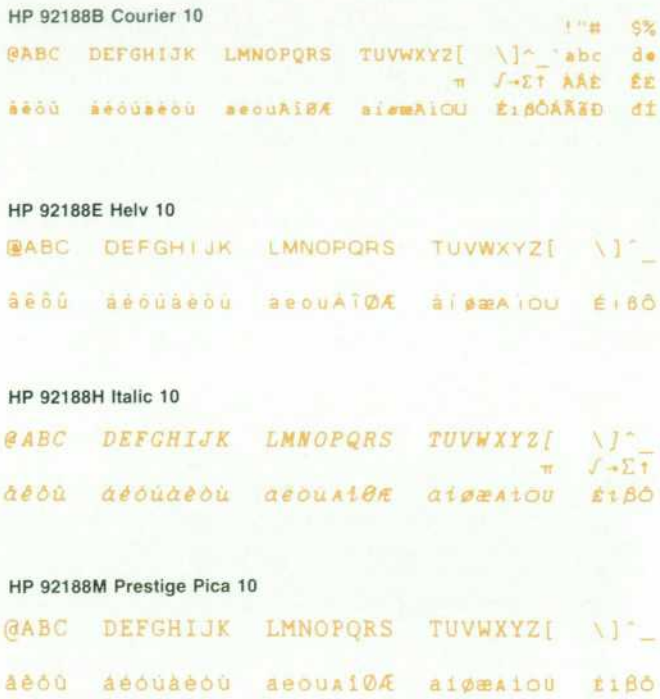


Fig. 5. *Examples of some near letter-quality fonts available for the HP 2934A Printer.*

if there is not a requirement for a dot at column four (strictly a function of the symbol to be printed), the next dot can be placed at any of the remaining positions in the cell.

As an example of this symbol definition criterion, Fig. 4 illustrates an uppercase Courier C. This symbol demonstrates the limits as explained above. In the second row there are four dots that must be printed for the upper portion of the symbol. The dot labeled A at position 10 is the first dot in the row and can be printed without restriction. The next two dots (B and C) must be located four logical columns apart. This can be seen on the background grid. The next printable position on this row is position 22, but the symbol does not require a dot there. However, the symbol does require a dot at position 25, which is seven positions from the last dot (C) that was fired and is therefore a printable position.

Acknowledgments

I would like to thank the HP 2933A and HP 2934A design team for an outstanding effort in meeting an aggressive schedule. My special thanks to Mike Ard for his diligence and perseverance and to John DiVittorio who held the mechanism to the accuracy required to print NLQ characters. My thanks to Donna Engholm, Greg Hillman, Trudy Kuehn, Dave Lee, Joe Liu, Tom Pritchard, and Mike Stein.

In addition, thanks to the HP 2932A team that provided the foundation for the HP 2934A: printhead designers Al Olson, Bill Stiggelbout, Charlie Knowles, and Kevin Kersey, print mechanism designers Jeff Grange, Alan Biggs, Olev Tammer, Chip Coffey, Chris Rasmussen, Warren Harwood, Ken Williams, and Steve Rasmussen, electronics designers David Parks, Steve Cobb, and Claude Nichols, and product designers Gene Jones, Don Bloyer, and Sohrab Vossoughi.

Custom IC Controls Dot-Matrix Impact Printers

This custom integrated circuit performs the complex logic required for controlling the printwires and the printhead carriage motor in a family of high-performance serial dot-matrix printers.

by Thomas B. Pritchard and David S. Lee

THE ELECTRONICS used in the HP 293X Printer family includes a custom integrated circuit to interface between the microprocessor and the printhead and its carriage motor. The special characteristics of the printhead require much parallel processing with timing resolution and accuracy down to one microsecond. In addition, the open-loop stepping of the carriage motor and the open-loop firing of dots are not performed at the same time, so a method of synchronization is necessary. These features cannot be implemented in a single general-purpose microprocessor and would be uneconomical if implemented with multiple parallel processors or discrete logic. A custom IC fills these requirements while providing many other beneficial features.

To illustrate the advantages of using a custom IC, Table I shows a comparison between the TTL breadboard used during development to simulate the custom IC and the custom IC itself. Not including the additional cost of a larger power supply, more bypassing, and the larger printed circuit board area, the production cost of the TTL implementation would have been 6½ times the cost of the custom IC, even after amortizing the development cost of the IC over the expected life of the product. Several other significant advantages of a custom IC are easier and faster testing, ability to choose a package pin configuration to minimize printed circuit board layout interconnect, and lower inventory parts count.

Table I

Comparison of Discrete TTL Versus Custom IC

	TTL	IC	Units
Number of ICs	296	1	
Total number of pins	4364	40	
Board space	1050	8	cm^2
Maximum worst-case power	13	0.6	watts

Circuit Requirements

Fig. 1 shows the operating environment for the custom IC. The inputs to the chip from the eight-bit 8051 microprocessor controller are a six-bit-wide data bus, a four-bit address bus, and a control bus. Outputs supplied by the chip are twelve printwire control signals sent to the printwire drivers and four-phase control signals sent to the printhead carriage motor.

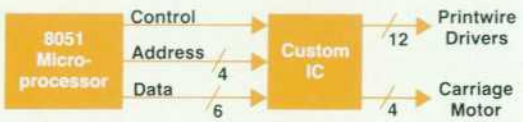
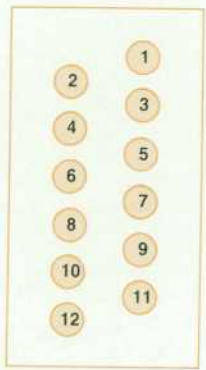
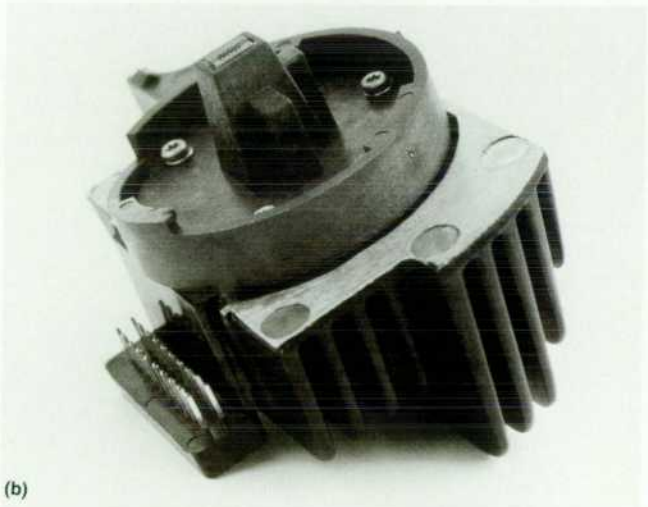


Fig. 1. *The custom IC used in the HP 293X Printers interfaces the controlling microprocessor in these printers with their printhead and its carriage drive motor.*



(a)



(b)

Fig. 2. *(a) Configuration of the printwires on the HP 293X printhead as viewed looking through the printhead to the surface of the paper. (b) Photograph of printhead.*

Fig. 2 shows the physical arrangement of the twelve dots on the printhead. The twelve printwires are arranged in two columns of six wires each. The dots made by one column are staggered vertically with respect to the dots made by the other column. One column consists of only even-numbered dots and the other column consists of only odd-numbered dots. Because of the separation of the two columns, a timing delay is required for firing the second column. For example, to print a vertical solid straight line on the paper when the printhead is moving from left to right, the odd-numbered column is fired first. Sometime later (depending on printhead speed), when the even-numbered column aligns with the previous position of the odd-numbered column when it fired, the even-numbered column is fired. Since the HP 293X Printers are bidirectional printers, the printwires are also activated when the printhead moves from right to left. In this case, the even-numbered column fires first and the delay is applied to the odd-numbered column.

Another requirement of the custom IC is data buffering. Consider when the printer starts from idle. The leading column of printwires begins to print first and at the same time the printhead advances. Because of the relatively wide horizontal separation of the two printwire columns, the leading column will have printed between two and eight times (depending on dot density and printhead speed) before the trailing column reaches the first firing position. Since the printing data is given to the chip one complete vertical line pattern (up to all 12 dots) at a time, it is necessary for the chip to be able to buffer up to eight columns of delayed data for the trailing printwire column.

Other printhead requirements are the maximum firing frequency and a dual-voltage, variable-length firing waveform. To produce high-resolution dot placement for near letter quality printing, but still not exceed the maximum firing frequency, a dot may only be fired at most every fourth possible firing time.

Fig. 3a illustrates the dual applied voltage waveform requirements. When initially turned on, the solenoid firing a printwire requires a short high-voltage pulse, called a kick pulse, to build up flux and get the wire moving toward the ribbon. Then the voltage is reduced to maintain the velocity of the wire. Before the wire hits the ribbon, at what is called the hold time, the applied voltage is turned off so the wire can bounce off the ribbon after impact. The wire cannot be fired again until it returns to its rest position.

An additional complication of the waveform generation occurs when the wire is fired at a high, but still allowable frequency. When the wire has just returned to its rest position, there is still residual energy in the system, composed of some magnetic flux remaining in the solenoid that fired the wire as well as some mechanical oscillation of the wire against its return stop. If the same firing waveform were immediately applied, the wire would strike the paper slightly early. Although the resulting dot placement error would be acceptable, this unfortunately would also result in too much energy delivered to the wire. The wire would strike the ribbon harder, leaving more ink on the page and producing inconsistent darkness of dots, which is unacceptable. In addition, this would prevent the wire from bouncing off the ribbon fast enough, and since the printhead is moving relative to the ribbon, the ribbon could tear. The chosen solution to the problem is to shorten the hold pulse width whenever the same wire was just fired a short time earlier. This can be seen in Fig. 3a by comparing the waveforms for wires one, nine, and eleven.

The printhead carriage motor in the HP 293X Printers is a unipolar four-phase step motor. To control the speed and direction of the carriage, the custom IC must supply the appropriate four phases to drive the motor. One of the requirements of the chip is that it be able to handle a wide range of printhead carriage speeds in both directions and yet require minimum attention from the control microprocessor. Another requirement is ramp-up and ramp-down timing. The stepping of the carriage motor must also be synchronized with the firing of the printwires. Because the carriage motor control is an open-loop system, this synchronization between the location of the carriage and the firing of the wires is crucial to eliminate cumulative errors.

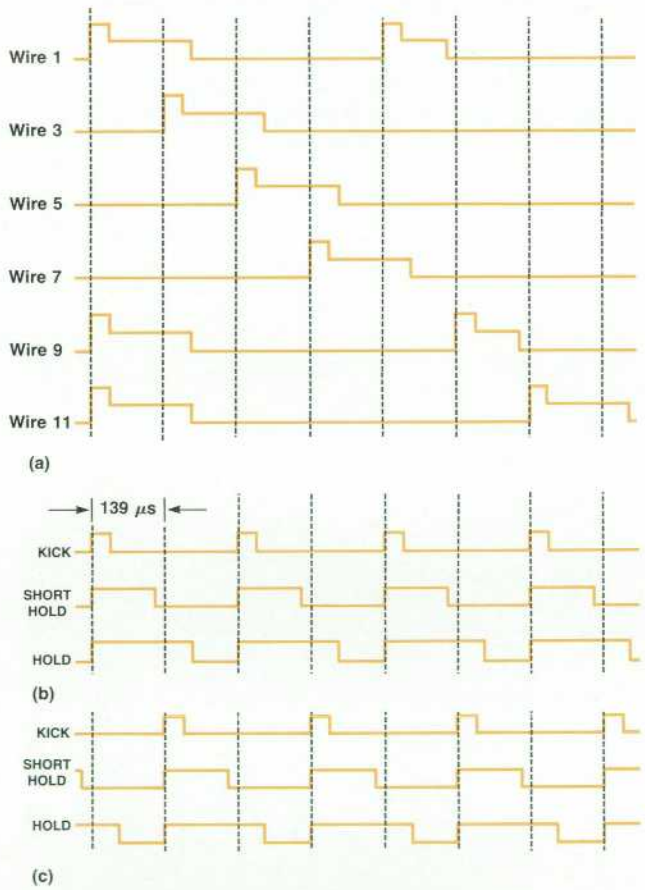


Fig. 3. *Typical firing and timing waveforms for the odd-numbered printwires in the right column (looking toward the paper). Note that each wire cannot be fired more than once every four intervals (139 μs per interval). (a) Firing waveforms. Note dual voltage levels and varying hold times (see text). (b) Timing waveforms for generator A (see Fig. 5). (c) Timing waveforms for generator B.*

Circuit Operation

Fig. 4 shows a block diagram of the dot input and carriage

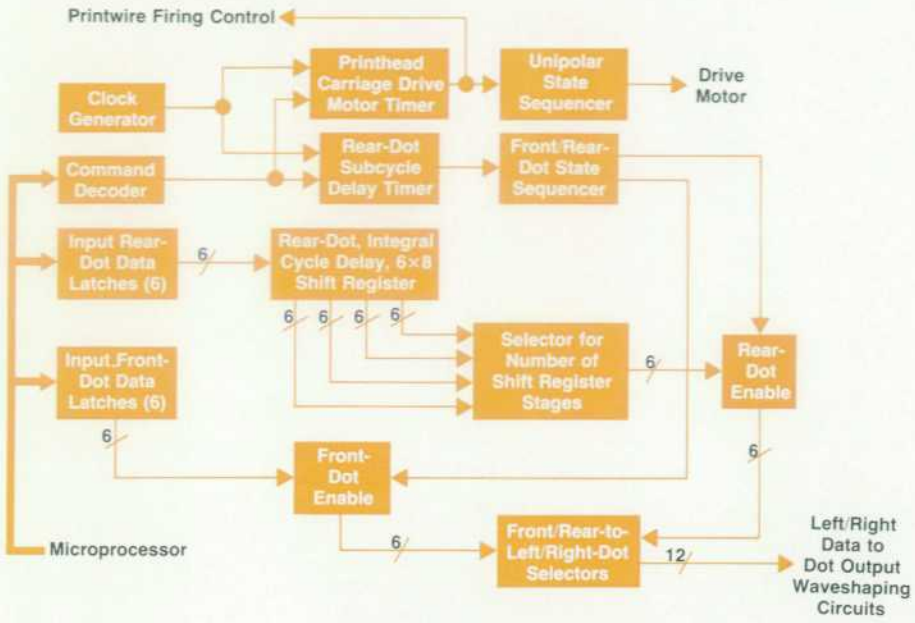


Fig. 4. *Block diagram of dot input and carriage motor control portion of the custom IC for the HP 293X Printers.*

motor control circuitry portion of the custom control IC used in the HP 293X Printers. As mentioned earlier, the dot data supplied by the control microprocessor must be buffered for the trailing column of printwires. Depending on the direction of the carriage motor, the data for the leading column is sent to the front-dot data latches and the data for the trailing column is sent to the rear-dot data latches and delayed by a shift register according to the horizontal dot density required. The front/rear-dot state sequencer then enables the leading and trailing column firing times according to the current carriage motor velocity.

The carriage motor control circuit consists of a four-bit state machine and an eight-bit-wide programmable timer. The output of the timer clocks the state machine, which generates the waveforms required by the carriage motor. The programmability of the timer allows a wide range of printhead velocities.

Since the printing mechanism is an open-loop system, a registration error might accumulate. This could be a significant factor affecting print quality, particularly when a long line is printed. The custom IC solves this problem by feeding the output of the carriage motor timer back to the printwire firing control circuit. Hence, the firing of the wires is synchronized with the steps of the carriage motor. In addition, to assure a consistent starting point at power on, the position of the printhead is initialized by driving it all the way to the right and then returning it to the left. If the printhead is in the middle of the line at power-on, it is still driven to the right as if it were at the start of the line. Since the carriage motor torque is limited, no damage is done by driving it against the right margin stop during this initialization.

Each signal indicating when each wire should be fired must be stretched from a one-microsecond pulse to the waveform required by the printwire driver as shown in Fig. 3a. Since the waveform generators require much silicon area, it was undesirable to have one for each of the twelve wires. Therefore, only four are used, and when a wire is fired, the custom IC selects one of these four waveform generators. The four generators are divided into two pairs, one pair for each printwire column of the printhead. This is necessary since the left column is fired asynchronously with respect to the right column. Within the right column pair of waveform generators, two circuits are needed to generate the necessary waveforms for the six wires as illustrated in Fig. 3. While normally only one of these two circuits might be expected to be needed because the 139-microsecond dot rate is already generated by the 8051 control microprocessor, two generators are required because the 8051's interrupt accuracy is not sufficient to control the waveforms to a resolution of one microsecond.

Fig. 5 illustrates the waveshaping circuitry for the odd-numbered (right) column. Identical logic circuitry is used for the even-numbered column. As a firing pulse comes in, the circuit checks to see which of the two timers is just starting its cycle and the data gets latched in the appropriate A or B hold-time flip-flop. The wire settling timers, one for each wire, indicate how long it has been since that same wire was last fired. The wire settling timers and the hold-time flip-flops combine the waveforms shown in Fig. 3b and 3c to generate the independent firing waveforms shown in Fig. 3a. The kick and hold data for each wire is multiplexed on the outputs to reduce the IC package size to 40 pins. The data is then externally demultiplexed and the actual 36.5V kick and 6.5V hold voltages are generated.

Since development of this IC was done in parallel with that for the printhead, not all of the characteristics of the head were known at the time. Because of this, it was necessary to make many functions programmable, including the kick, short-hold, and hold times. In the final implementation, the kick time is varied by the firmware, the value being a function of the power supply voltage. However, the short-hold and hold times, once programmed during initialization, are constant.

Because of the rubbing of moving paper, printhead, and ribbon, and because of frequent user interaction, electrostatic discharge (ESD) is a common problem in printers. If, because of ESD, a microprocessor is allowed to send illegiti-

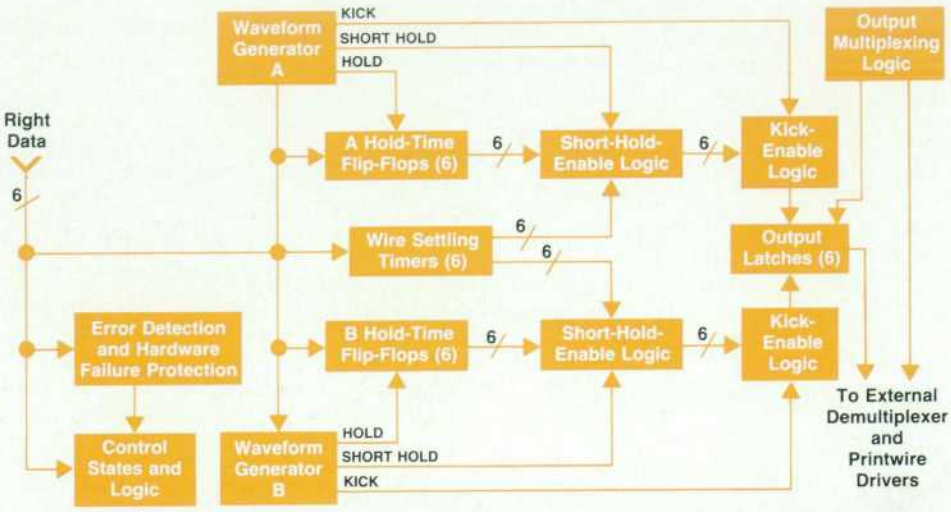


Fig. 5. *Block diagram of dot output waveshaping portion of the custom IC for the right (odd-numbered) column of printwires.*

mate commands, it may cause a hardware failure in the electromechanical system and may require a service call. To reduce the possibility of this happening, the custom IC will reset itself if it detects certain fault conditions.

Implementation

The first step in the implementation of the custom chip was the development of a TTL IC simulator. This enabled the firmware engineers to start working before the IC fabrication was done, and also provided feedback for necessary design changes because of unexpected system characteristics. For example, the original breadboard did not perform the short-hold function; it was well into the project when it was decided that the IC design should be changed to incorporate this feature. The original breadboard was wire-wrapped; the later simulator used stitch-wire connections.

A proprietary NMOS process developed by HP was chosen based on economic considerations. A standard cell approach was used as the best compromise in this project between IC manufacturing cost and development time. The die, which measures 6440 μm by 6250 μm, is mounted and bonded in a plastic dual in-line 40-pin package.

The proprietary HP software development tools and design processes used to generate this custom IC included schematic capture, evaluation, logic verification, fault simulation, automatic placement and routing, timing simulations, and test pattern generation. The schematic capture, evaluation, and timing simulations were performed on HP 2647A Graphics Terminals using an HP 3000 Series 68 Computer. The logic verification, fault simulation, and test pattern generation were performed on HP 2647A Terminals using an HP 1000 E-Series Computer. The automatic placement and routing were performed on an Amdahl 470.

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