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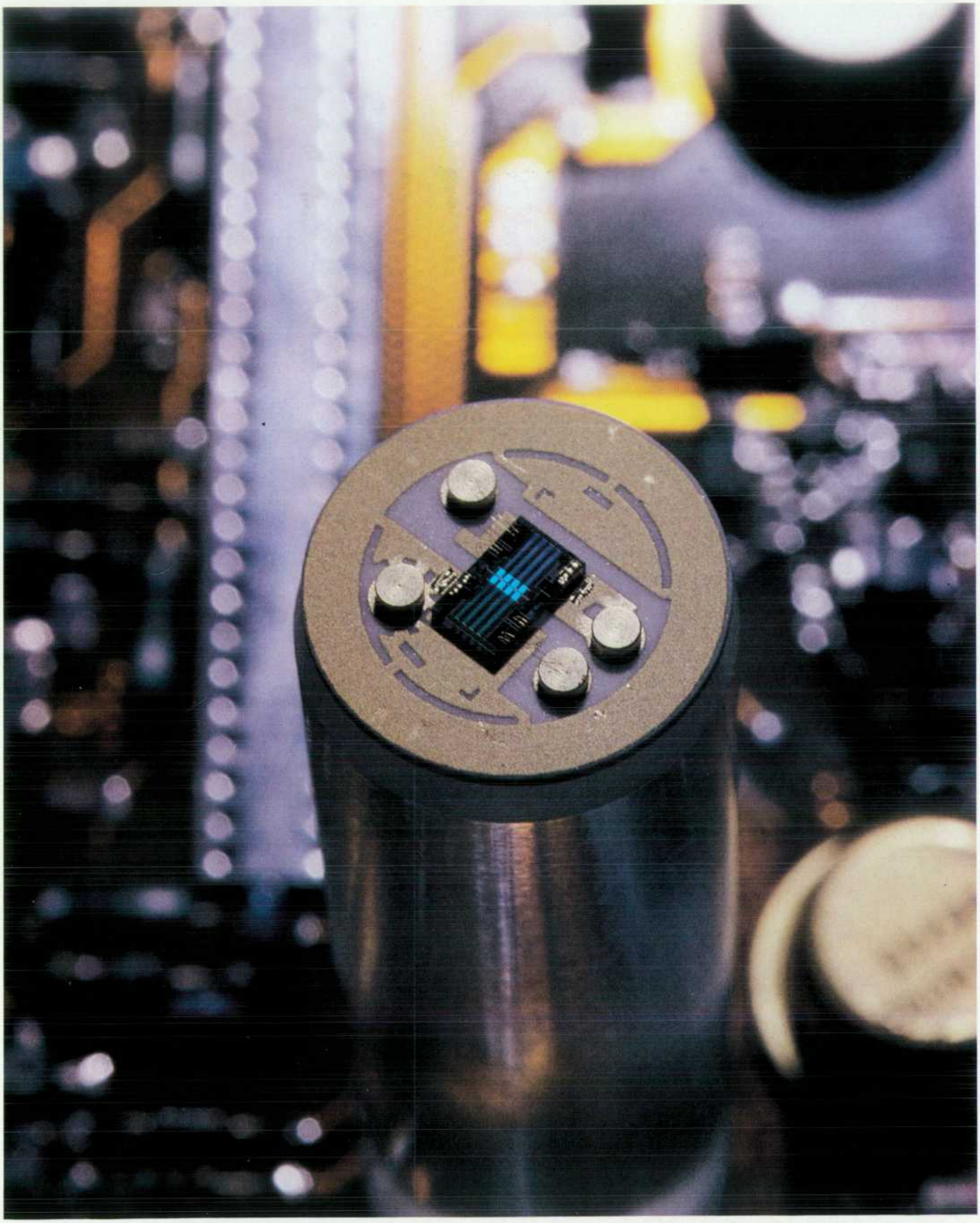

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Articles

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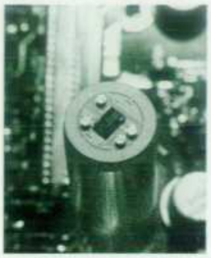
In this Issue



The object on top of the acrylic rod in the center of our cover photo is a surface-acoustic-wave resonator (SAWR), one of several that are important contributors to the high performance of a new synthesized signal generator, the HP 8642A/B. This RF signal source is designed to produce exceptionally clean signals at frequencies from 100 kilohertz to 1057.5 megahertz (A model) or 2115 megahertz (B model). Sources like the HP 8642A/B are needed for testing the vast array of equipment operating in this frequency range, including RF communications systems like the new cellular radiotelephones, home entertainment devices, and avionics equipment such as instrument landing systems (ILS). In the design and production of RF communications equipment, for example, the signal generator simulates an ideal transmitter for making measurements on receivers. The critical signal generator specifications are level accuracy, phase noise, and spurious outputs, because these characteristics have a direct impact on measurements of the critical receiver characteristics of sensitivity, selectivity, and spurious response. The HP 8642A/B's performance in these key areas, say its designers, is the best available today. You'll find an introduction to the HP 8642A/B in the article on page 4. The other six articles in this issue deal with its contributions to the state of the art in its electrical and mechanical designs, simplified control and operation, automatic test system compatibility, and simplified repair and calibration.

SAW devices first appeared in these pages in December 1981. In February of that year, our issue was devoted to the HP 8662A Signal Generator, an RF signal source designed for exceptional spectral purity, like the HP 8642A/B, and very fast frequency switching speed. It's instructive to compare these two designs, which are rivals for the best-spectral-purity award. Of course, the newer generator takes advantage of five years of technological development, including the SAWRs. However, both designs depend on multiple phase-locked loops and special low-noise oscillators (a switched-inductance design in the HP 8662A). The HP 8642A/B doesn't eliminate the need for the HP 8662A, but it may well unseat the long-established low-phase-noise standard, the HP 8640B. This 13-year-old design, featured in our February 1973 issue, is mechanically tuned and can't match the production testing speed of the newer generators. The HP 8662A is best for phase noise closer than 5 kHz to the carrier and for fast switching, characteristics that are important in satellite and radar testing, where the carrier gets multiplied to microwave frequencies. The HP 8642A/B is best for phase noise at offsets greater than 5 kHz, has the lowest spurious outputs, and costs less than the HP 8662A. Its characteristics are important for RF communications testing, where adjacent channel noise is critical. The HP 8642A/B's phase noise characteristics are similar to but about 6 dB better than those of the older HP 8640B.

December is our annual index issue. The 1985 index begins on page 36.

-R.P. Dolan

What's Ahead

Leading off next month's issue is our second article on HP's next generation of computers now under development. The article discusses the fundamentals of the optimizing compilers developed for the new computers' reduced-complexity architecture. Other articles will cover the design of the HP 7090A Measurement Plotting System, which is a waveform recorder, X-Y recorder, and digital plotter all in one unit, and usability testing of the HP Portable and Integral Personal Computers.

A High-Performance Signal Generator for RF Communications Testing

High-reliability design, extended calibration intervals, and fast calibration and repair maximize ATE system uptime. Spectral purity is exceptional.

by Robert E. Burns

AS THE COMMUNICATIONS SPECTRUM becomes increasingly crowded, requirements for the equipment used in communications systems become more stringent. The advent of new methods for people to communicate using radio frequencies, such as cellular radio, accelerates this trend. Manufacturers of communications equipment need calibrated signals of high quality to verify that their products are meeting stringent specifications. This needs to be done quickly, usually under computer control. The HP 8642A and 8642B Signal Generators (Fig. 1) can provide these signals.

High-quality communications equipment must transmit and receive voice and other data clearly and accurately over long distances, sometimes in the presence of strong interference at nearby frequencies. To the radio manufacturer, this means that the receiver must be sensitive to very small or weak signals. The noise the receiver adds must be small. The receiver must be able to demodulate the data with low distortion. It must also reject all frequencies other than the one it is tuned to.

To test these receiver characteristics, low-noise signals are required whose amplitude and modulation characteristics can be controlled precisely over a wide dynamic range. The HP 8642A/B can provide signal levels from −140 dBm (0.023 μV) to +20 dBm (2.24 V) with 0.1-dB resolution and guaranteed accuracy of ±1 dB above 0.1 μV over the specified environmental conditions. The frequency range of the HP 8642A is 100 kHz to 1057.5 MHz, and the HP 8642B generates frequencies from 100 kHz to 2115 MHz. Both models have a built-in modulation oscillator that generates signals from 20 Hz to 100 kHz. Hence the HP 8642B, with its internal modulation oscillator, can generate frequencies from 20 Hz to 2115 MHz. This represents a dynamic range of eight orders of magnitude for both frequency and amplitude control. In both models, output can be swept in both frequency and amplitude. AM can be controlled from 0 to 99.9% with 0.1% resolution. The output signal can be frequency modulated to deviations beyond 375 kHz at any carrier frequency (provided that the instantaneous frequency is always above 100 kHz). Phase and pulse modulation are also available.

Perhaps the greatest performance contribution of the HP 8642A/B is its exceptional spectral purity at offsets important in communication systems. The single-sideband (SSB) noise of −138 dBc/Hz at an offset of 20 kHz from a 1-GHz carrier is further lowered using binary frequency dividers for output frequencies down to 100 kHz, providing exceptionally clean performance throughout the RF spectrum. But low noise is not useful if large spurious signals are present. All HP 8642A/B nonharmonics are guaranteed to be below −100 dBc. Attention has been paid to other important details, such as radiated emissions and third-order intermodulation performance, ensuring exceptional out-of-channel performance. Thus the HP 8642A/B can offer in a fully programmable instrument the level of measurement confidence normally associated only with manually controlled cavity-tuned generators.

Fig. 1. *The HP 8642A/B Signal Generator uses new low-noise oscillator designs with high-Q surface-acoustic-wave (SAW) resonators to improve spectral purity over cavity-tuned generators. Its frequency range is 100 kHz to 1057.5 MHz (A model) or 2115 MHz (B model). High accuracy, wide output power range, and broad modulation capabilities make it suitable for the most stringent receiver tests.*

These characteristics allow radio manufacturers to measure receiver parameters with high accuracy and confidence. The signal generator can be tuned to the same frequency as the receiver to make in-channel measurements such as sensitivity, SINAD (ratio of signal level to noise and distortion), flatness, and distortion. The accurate frequency, output level, and modulation characteristics of the HP 8642A/B reduce errors in these measurements. The superior spectral purity of the HP 8642A/B allows accurate measurements of the receiver's ability to reject interference (out-of-channel measurements). In this case, the signal generator is tuned to a frequency different from the frequency the radio is receiving. The extremely low levels of noise and spurious signals of frequencies other than the HP 8642A/B output frequency means that very little power is generated in the channel the receiver is tuned to. This is important if the receiver's ability to reject interference, or selectivity, is to be measured. These same high-performance characteristics are also useful in general-purpose RF applications.

System Architecture

The design that provides this level of performance in a synthesized, fully programmable signal generator begins with the overall block diagram, Fig. 2. The HP 8642A/B is an indirect frequency synthesizer employing phase-locked loops for frequency control and modulation. The design of any phase-locked loop involves complex trade-offs among many different performance parameters such as frequency resolution, switching speed, spectral purity, and modulation characteristics. The HP 8642A/B block diagram separates these often conflicting challenges into three separate phase-locked loops. Each loop is designed to optimize a particular parameter, and these characteristics remain relatively unaffected by changes in the output frequency. Two other loops are used to combine these three separate signals into one continuous output signal covering the main octave of operation from approximately 0.5 to 1 GHz. A sixth loop provides reference frequencies. The design of the six phase-locked loops in the HP 8642A/B is discussed in the article on page 24. The output sections and the audio modulation facilities are described in the articles on pages 18 and 31.

Designing for the ATE Environment

Providing the full capability of the HP 8642A/B block diagram to the user in a straightforward and friendly manner proved challenging. A 16-bit microprocessor accessing over 250K bytes of memory is used to achieve this objective. An LCD display was selected to provide alphanumeric capability without strobe-related electromagnetic interference. Extensive help firmware uses the display to lead even first-time users through subtle aspects of instrument operation.

Besides setting new standards for RF performance, the HP 8642A/B is designed specifically for the ATE (automatic test equipment) environment. Ease of configuration, reliability, and uptime have become as important in buying decisions for this type of equipment as the traditional concerns of price and performance. The presence of a powerful internal controller, coupled with modular mechanical design, allowed the design team to address these challenges in new ways. The controller design is discussed in the article on page 6.

A typical application for the HP 8642A/B may put this instrument in a complex system of instruments represent-

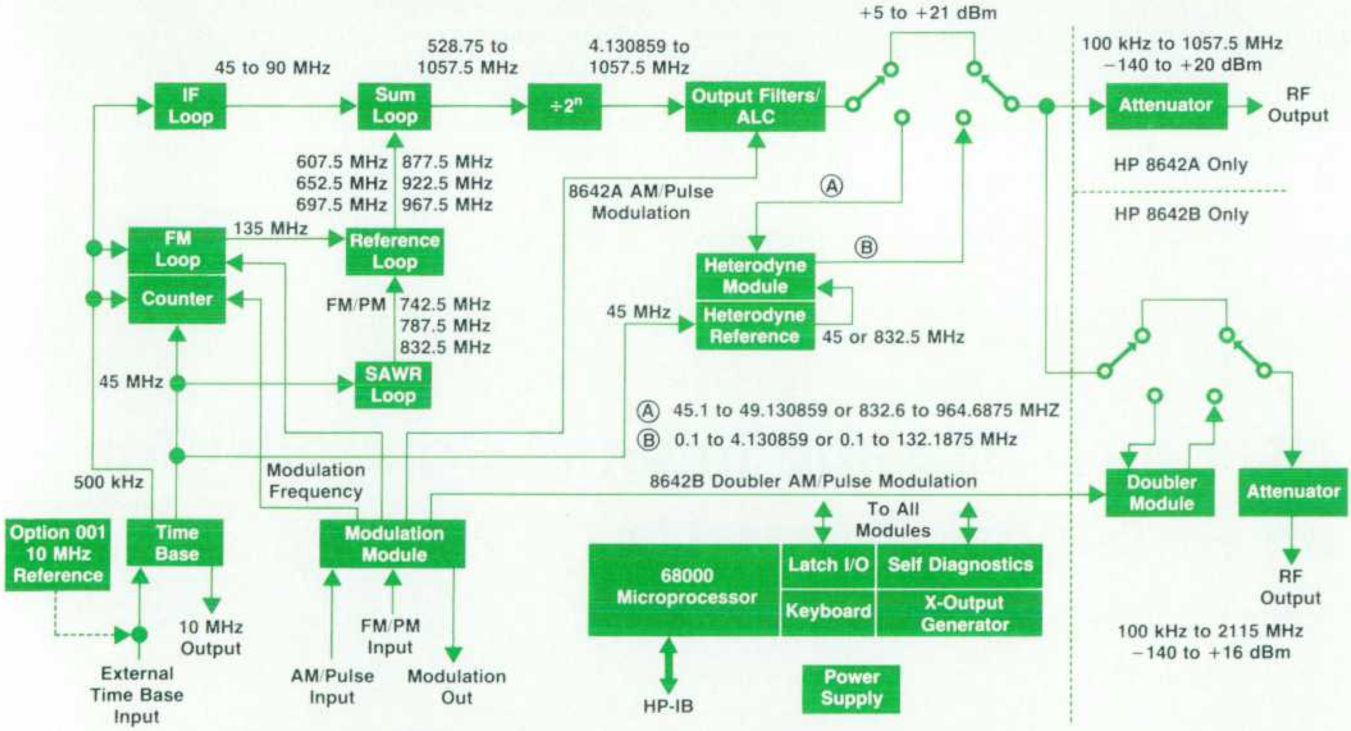


Fig. 2. *The HP 8642A/B is an indirect frequency synthesizer. Six phase-locked loops are used for frequency control and modulation.*

ing large investments in equipment and engineering. High uptime, the percentage of time the instrument is not down for troubleshooting, repair, or calibration, is important for the user to benefit fully from the investment made in a complex test system. High uptime starts with good reliability. During development of the HP 8642A/B, this meant extensive stress analysis of all components, junction temperatures analyzed and minimized, and copious amounts of air flow provided. Development hardware at every phase was subjected to extensive stress testing involving thermal, mechanical, and electrical shock.

Given a collection of over 3000 electrical components, however, the likelihood of failure can be minimized but will still remain finite. Clearly there are advantages to going beyond designing for reliability and considering the design impacts on diagnostics, troubleshooting, and repair. Key to easy serviceability is a mechanical product design that allows easy access to critical circuitry. This objective is usually at odds with the packaging requirements of a synthesizer having a −100 dBc specification on spurious outputs, where often the first impulse is to weld it shut. In the HP 8642A/B, a clamshell die-cast housing maximizes the grounding area available for low-pressure gasketing. This, coupled with the rigidity of the die-cast housings, minimizes the number of fasteners required to seal a module. All RF circuitry is housed in one of eight die-cast modules. These modules have well-defined specifications on all inputs and outputs. They can be individually extended quickly and easily by releasing two snap fasteners. By removing typically six to eight screws, large sections of critical circuitry can be exposed and analyzed while operating. Details of the mechanical design are in the article on page 14.

This sort of accessibility is only valuable if a fault can be quickly traced to an individual module. To achieve this goal, basic test equipment such as a voltmeter and a power meter are built into the instrument. Each module contains an analog multiplexer that allows access to several critical monitoring points, yet adds only one filtered line to the module. These points are polled and monitored through several different levels of diagnostic tests. Critical failures, such as loop unlock, are monitored continuously. Extensive diagnostic firmware allows the operator to trace most faults to the module level without removing the instrument covers. If maximum system uptime is a must, a failed module can simply be exchanged with a new module in minutes. An EAROM sent with the new module can be downloaded into instrument memory quickly and easily, bringing the instrument into calibration without the need for any manual adjustments. If component-level repair is more appropriate, the built-in diagnostics can help track down the faulty component. If it becomes necessary to replace a critical component, the HP 8642A/B can recalibrate itself automatically. Acting as an HP-IB controller, it can direct certain pieces of associated test equipment to make measurements, then store the new calibration data internally. Using these features, engineers were able to trace induced faults in developmental HP 8642A/Bs over the telephone using modems.

The serviceability approach taken for the HP 8642A/B is discussed in the article on page 10. Built upon a foundation of high reliability, these diagnostic and serviceability features should contribute to saved time and money for designers of RF test systems.

Acknowledgments

Many people contributed to the HP 8642A/B project over a number of years, making it impossible to mention all of the key people here. Fundamental to the development of this product were the design engineers who are represented as authors in following articles. Also worthy of mention are the contributions of Tim Carey, Fred Ives, and Roger Muat to the original block diagram design. Rob Oeflein and John Richardson helped refine the product concept. Early design decisions benefitted from inputs from Steve Holdaway and Mike Hadley. Eric Anderson and Jon Sigler achieved the amazing feat of maintaining unyielding positions on product reliability and serviceability without creating enemies. Efforts well beyond the call of duty were turned in by Morris Chase, technician, and Billy Reynolds, tooling engineer. And finally, the entire group was orchestrated through the critical phases by Art Upham, program manager extraordinaire.

User Interface and Internal Controller for an RF Signal Generator

by Albert Einstein Lassiter and Charles R. Kogler

THE USER INTERFACE of the HP 8642A/B Signal Generator is designed to provide many conveniences and to make the instrument easy to use. The user interface includes the keyboard, the display, and the HP-IB (IEEE 488) interface.

The HP 8642A/B has a 25-character alphanumeric display for function settings and messages (see box, page 9). The instrument prompts the user with what is expected next in many cases so the operating manual doesn't have to be depended upon so heavily. Messages tell the user what is going on or what the user has done wrong. For example, AM TURNED OFF is displayed if AM is on when pulse modulation is selected. This message helps the user learn that AM can't be done simultaneously with pulse modulation. Another example is AMPTD LIMITS MAX AM, which tells the user that the requested AM setting is not allowed at the current amplitude setting.

Two user-defined displayable messages can be used for any desired purpose. These messages allow the display to be used as a test system's large-character display for prompting the operator, or for recording a company's capital asset number for the instrument inside the instrument, or for any other user-defined message. These user-defined battery-backed-up messages can be kept and displayed on demand, or output over the HP-IB.

All individual indicators outside the display have been eliminated by using the alphanumeric display. Individual indicators like SHIFT, RF.OFF, and PULSE simply appear in the alphanumeric display, thereby reducing the cost and clutter of the front panel. By using the alphanumeric display and by using individual LCD sigments as one-word indicators, about 40 individual indicators were eliminated.

A pull-out card is sometimes provided in other instruments to supply lists of message codes, HP-IB codes, and special functions. The need for a pull-out card has been eliminated by using the alphanumeric display and by printing HP-IB codes for all keys on the front panel near each key. The list of special functions is scrolled through on the display using the HELP function; since all messages are alphanumeric, there is no need to list the special functions on a pull-out card.

HP 8642A/B messages have a message code at the right end of each message (for example, E24 in the message AMPTD LIMITS MAX AM .E24). This message code allows easy reference to the operating manual, where each message is described more thoroughly. These descriptions are useful to those unfamiliar with the full meaning of messages and the abbreviations used within messages, and could be especially useful for nonEnglish-speaking users. Most of the descriptions of messages include a statement of what caused the message and what to do about it.

Built-in Convenience

The **OFF ON** key is used to toggle functions off and on. This key reduces the number of keys and the number of individual indicators needed for functions, and presents to the user a consistent, easy-to-understand method for turning functions off and on. This key is also used to recover from errors caused by accidentally hitting the wrong keys. Functions can be turned back on easily to their last selected values.

Amplitude can be set directly in units of dBm, volts, mV, μV, and dBμV. It can be set in other units, like dBV, dBmV, dBf, and dB relative to an arbitrary amplitude setting, by using the amplitude relative capabilities of the HP 8642A/B. The HP 8642A/B can also convert amplitude settings to any other amplitude units. For customers working in EMF amplitude units (popular in Europe and Japan) the HP 8642A/B has an EMF mode that causes all amplitude settings to be displayed and entered in EMF amplitude units (like EMF V, dB EMF μV, and so on). Once the amplitude units are configured, the user only needs to press one amplitude units key to terminate a new amplitude setting.

The knob functions on the HP 8642A/B are designed to provide conveniences to the user in setting functions. The knob can be used with any of the instrument's function settings, for manual sweeps, for scrolling through the list of special functions using the HELP function, or for changing the phase of the RF output in 1° steps. Each function also has its own settable increment value, which can be used with the **STEP** ⇧ and **STEP** ⇩ keys, or with the knob during the KNOB INCR mode. For instrument settings, when the knob is turned quickly, larger steps are taken, so the setting changes much more quickly. The knob algorithm allows the user to have control over three and sometimes four digits without having to change the knob resolution. This algorithm allows the user to go all the way from the minimum setting to the maximum and back in a relatively small number of turns. Once near a desired setting, turning the knob slowly gives precise steps of single digits to fine-tune the setting. The KNOB INCR mode allows the customer to define the size of each step. This mode can be used for putting (frequency) channel spacings on the knob so that each step from the knob gives the next channel. The KNOB HOLD function allows the knob to be dedicated to one function, while any other function is changed with the **STEP** keys and the **DATA** keypad. This function can be used to change frequency with the knob while changing amplitude with the **STEP** keys. The KNOB HOLD function can greatly reduce keystrokes when changing two parameters interactively.

The HP 8642A/B has 51 nonvolatile save/recall registers, which save all instrument settings, special functions, knob resolution, and other data. The recall registers can be used to make complicated instrument setups quickly and easily, to select the user's favorite modes (like EMF units, FM preemphasis, etc.), or just to make automatic testing work more quickly (RECALL is faster than setting states over the HP-IB). SAVE and RECALL can be used with the **STEP** ⇧ and **STEP** ⇩ keys to set up or modify sequences of recall registers, or to recall the last state recalled before the instrument's state was modified. The SEQuence function steps through instrument setups saved in consecutive recall registers. This function is especially useful in semiautomatic systems; an operator can sequence through up to 51 different states while testing or adjusting another unit under test.

HP-IB Design

The nonvolatile HP-IB address is settable from the front panel. To keep the instrument usable in a system even if the battery is dead, an internal switch will be read at turn-on if the address is lost.

The HP-IB status byte is designed so that it can be used flexibly during either status polling or when a service request (SRQ) causes an interrupt to a program. Of particular interest is how the HP 8642A/B communicates messages to the HP-IB controller. Three groups of messages are internally kept track of for possible HP-IB output. *Parameter changed* messages inform the user that the HP 8642A/B has changed some other setting to allow a new setting.

Execution error messages describe the HP 8642A/B's reason for not executing an attempted setting. *Hardware error* messages signal the presence of an internal hardware problem that the user might be able to resolve. There are separate status bits and message lists, and separate functions to clear the status bits and read back the messages for each of these three groups of messages. This separation provides enough flexibility to allow the HP-IB user to decide what types of messages to handle or ignore and when to handle them. For example, the user may want to ignore parameter changed messages, handle execution error messages by polling the status byte, and handle hardware error messages by having SRQ cause an interrupt.

Messages can be output as message code numbers (for easy comparison by a computer) or as alphanumeric strings (for message handling by a human or for output to a printer). The ability to output messages as alphanumeric strings can eliminate the need to look up message code numbers when developing a program.

The settings of functions are easily read over the HP-IB using the output active function (OA) command. The setting is output as a string that includes the function prefix and units. This string can be read directly into a numeric variable on an HP-IB computer or it can be read into a string variable which can be later written back to the HP 8642A/B to get that setting again. The string can be used to print the instrument's settings on a printer. As a convenience to users of a particular set of amplitude units, amplitude settings are output in whatever units they are set in (e.g., dB EMF μV or dB relative to the amplitude reference). The display can be read over the HP-IB, including cursor positions and the state of the display indicators below the alphanumeric characters. By reading the display, the states of modulation sources, special functions, increment set values, references, and so on can be read via the HP-IB.

The HP-IB interface, combined with the powerful service and diagnostic functions (see article, page 10), results in very powerful, useful, and time-saving capabilities available in no other signal generator.

Internal Controller Design

Radio frequency (RF) signal generators are primarily analog instruments, and in the past, their design has been in the analog RF designers' domain. When microprocessors were first used in instruments, their main purpose was automating functions, so the instrument could be used in an automatic test equipment (ATE) environment. The role of the microprocessor has been carried much farther during the development of the HP 8642A/B.

From the very beginning of the project, the analog designers were encouraged to consider the microprocessor an integral part of their design, and to make use of it to the fullest. The digital hardware/firmware team demonstrated its commitment to this philosophy by selecting a 16-bit 68000 instead of a less powerful 8-bit microprocessor. The implementation of this design philosophy has resulted in a very high degree of microprocessor interaction with the analog hardware, and provides the customer higher performance, better reliability, and more functionality for lower cost.

The digital hardware/firmware design team had several key goals. Maximum performance and functionality were needed. The internal controller had to provide what was needed for the instrument's modules to meet their particular input and output specifications. The complicated set of signal generator hardware and capabilities had to be presented in a friendly, easy-to-use manner.

Extensive serviceability-related built-in features such as module swap, self-calibration, and self-diagnostics were to be implemented to maximize the uptime of the instrument and to reduce costs during production (see article, page 10).

The power of the microprocessor made possible a wide range of easy-to-use functions that provide additional useful instrument capabilities. These capabilities are implemented totally or mostly in firmware, using hardware that is already required to perform some other function. For example, stepped frequency sweep, phase-continous frequency sweep, and amplitude sweep are implemented in firmware. The only hardware added for these sweeps is a DAC (digital-to-analog converter) for the X-axis output, an output line for the Z-axis output, and one extra control line for the IF reference loop. Special functions to set frequency to 0.1-Hz resolution, to change the output phase in one-degree steps, to invert the polarity of the external FM/PM input, to disable settling (for faster switching), and to hold the attenuator setting during amplitude setting changes are implemented with no additional hardware. The RF OFF/ON function (which reduces the RF level without switching the attenuators, thereby prolonging attenuator life) requires no additional hardware, because it uses a combination of filter and divider switching and reduction of the output section vernier level. The dcFM update mode special function (which shows frequency drift on the display during dcFM) uses hardware already required for doing dcFM correction.

The HP 8642A/B hardware is rather complicated, with many instances of coupled functions. That is, the range of one function's settings may be limited by the settings of other functions. Range checking of functions is optimized to allow the user to get the maximum performance and flexibility from the instrument. An example of this flexibility is the coupling between the amplitude and AM settings. At amplitudes above 14 dBm, it is not possible to get the maximum AM depth of 99.9%. The combination of amplitude and AM settings is limited such that the output is limited to a maximum peak envelope power of 20 dBm. Thus, at an amplitude setting of 15.8 dBm, the user is allowed to set AM as high as 62.2%. Conversely, if the user has AM set to 30%, the instrument allows the amplitude to be set up to 17.7 dBm. More complicated examples of coupled functions are the relationship between RF frequency, FM, modulation frequency, and the FM preemphasis special function, and the relationship between center frequency, sweep span, and sweep time for phase-continuous frequency sweep. Again in these cases, the user is allowed the maximum possible performance for all combinations of the coupled functions.

The microprocessor controls and reads over 300 bits of instrument hardware information. Of these, about 250 bits relate to analog hardware control and feedback. The processor is especially interactive with the modulation oscillator. Normally, the microprocessor counts the modulation frequency and feeds back correction data to the oscillator hardware. This processor interaction enables the instrument to meet its stringent specifications for modulation oscillator accuracy without resorting to a synthesized modulation source and associated spurious outputs. This correction process can take up to 250 ms. For faster tuning speed, a special function that disables this counting and correcting for each modulation oscillator change can be used. Correction data from the previous counting and correcting cycle is used instead. Since the amount of drift over time is relatively small, the user can calibrate the settings when a test begins by using the count and correct algorithm (or the user can use a different special function that calibrates all five modulation oscillator bands at once) for the first setting(s) of the modulation oscillator, then switch to the other algorithm with negligible loss of accuracy, but with much faster switching time.

Heavy processor interaction with analog hardware is also used during dcFM (see article, page 24).

Acknowledgments

Mike Wende also worked on the design of the controller hardware. We would like to thank Art Upham for numerous and invaluable contributions. Lynn Wheelwright supplied and supported our firmware development tools. Morris Chase gave us many valuable suggestions about both

Display Design

In designing the HP 8642A/B display, several key goals had to be met. The instrument state information had to be presented understandably with minimum clutter so that the instrument would be easy to use. The volume available inside the instrument for the display and keyboard was very limited. The display had to meet military viewing angle specifications and had to be viewable in dim lighting. It had to generate very low electromagnetic interference (EMI), and power consumption had to be low. The tradeoffs clearly showed that a custom alphanumeric liquid-crystal display (LCD) was the best way to meet the objectives.

Seven-segment light-emitting diode (LED) displays were found to draw too much current (over an ampere would be needed). Using that much current would make the power transformer large enough to require the next larger cabinet size. Because of the stringent EMI specifications, LEDs could not be driven multiplexed to reduce power consumption. Other types of displays, like CRTs, vacuum fluorescent, and so on, require too much power, use too much instrument volume, or generate too much EMI.

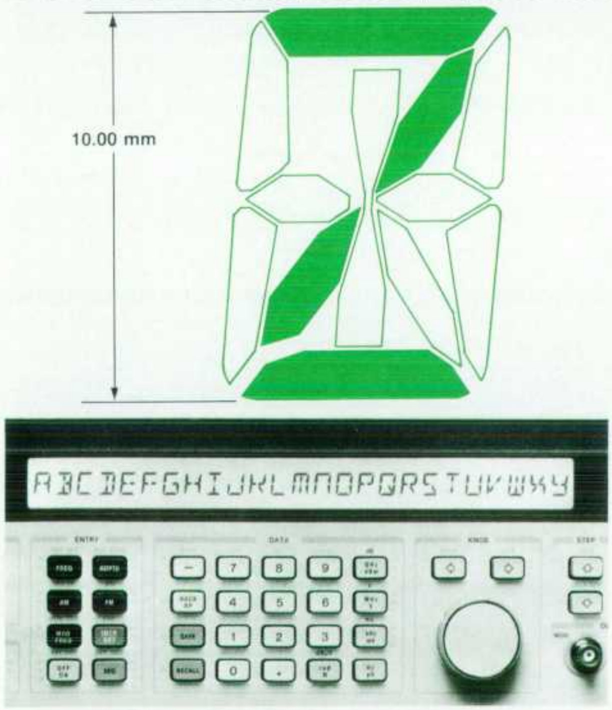


Fig. 1. *The HP 8642A/B's 11-segment character (a) and character set (b) were developed to reduce the number of LCD driver pins without resorting to multiplexing.*

A liquid-crystal display allows the use of alphanumeric characters for the display of messages, prompts, and other information, uses a small amount of instrument volume, and uses very little power (only milliamperes including drivers). In addition, LCDs cost less than LEDs, there are no alignment problems with the individual display elements, and LCDs allow much more flexibility for displaying information to the user.

We needed a way to drive the LCDs to get the best viewing angle for our application. LCDs have a viewing angle limitation that depends on the peak voltage applied between the backplane and the individual segments. The larger the voltage used to drive the LCD, the better the viewing angle is.

LCDs with many segments are usually designed with multiple backplanes so that the segments are actually driven with multiple-level multiplexed waveforms. When LCDs are driven multiplexed, off segments aren't really driven at zero volts, but only at a low enough voltage so that they do not look turned on within a certain viewing angle. This multiplexing therefore limits the drive voltage of the on segments to about 3.2V peak for the type of LCD used in the HP 8642A/B. Below 3.2V the viewing angle is fairly limited. Above 3.2V the off segments start to look slightly on.

To get the best possible viewing angle, the HP 8642A/B LCD segments are driven with no multiplexing, which allows segments to be driven at 5.2V peak (10.4V peak-to-peak) with the off segments driven at zero volts. The 5.2V power supply is already available for the digital ICs. Driving the LCD with no multiplexing requires many more LCD segment pins, which means more LCD driver ICs. To reduce the number of segments, an 11-segment character and character set are used instead of the more common 14-segment character and character set. This makes it possible to drive the 25-character display with just 11 LCD drivers (each driving 32 segments) instead of approximately 15.

Fig. 1 shows the 11-segment character and character set. Note that the center segment of the Z character is really just one segment, even though it appears to be two. The two sections are connected by an internal trace.

Some customers require the display to be readable in a dimly lit environment. LCDs are passive displays, so they need external lighting to be visible in dim light. A backlighting bar evenly lights the display using just two incandescent light bulbs, one at each end of the display. For better reliability the light bulbs are driven at well below their rated voltage.

The HP 8642A/B display is designed to be viewable in a 45° viewing cone even in the dark. The backlighting bar design is described in the article on page 14.

hardware and firmware related issues. Ken Burden modified and helped support our firmware development tools. We would especially like to thank Jena Pittmon and the rest of the technical writing staff for doing such an excellent job in writing the Operating Manual and Operating Fundamentals. These are our best manuals to date and are being used by other divisions as models for how to do instrument manuals. We would like to acknowledge the efforts of the entire HP 8642A/B production line for bringing problems to our attention promptly and for really taking the quality commitment to heart. We would also like to acknowledge the materials purchasing and scheduling groups and the components engineering group for sustained, high-quality efforts over a long period of time. Finally, thanks to the rest of the HP 8642A/B design team for their efforts in making our job easier.

Signal Generator Service Features Maximize Uptime

by Michael T. Wende

TO MAXIMIZE UPTIME, the HP 8642A/B Signal Generator is designed with an emphasis on reliability and extended calibration intervals, so that the intervals between failures or required calibrations are expected to be much longer than in previous generations of HP RF signal generators. To reduce downtime when calibration or repair does become necessary, the instrument has extensive built-in self-tests and service features for fault detection, fault diagnosis and isolation, and calibration. The fault detection facilities increase measurement confidence and reduce the time required to locate and fix system problems. The fault diagnosis and isolation facilities quickly isolate problems to one of the HP 8642A/B's independent modules, which can then be replaced easily on-site and recalibrated in minutes without the need for test equipment. Component-level repair and calibration of individual modules is addressed by other built-in features, including signature analysis, self-calibration routines requiring a minimum of additional equipment, and external automatic calibration capabilities.

Fig. 1 shows typical HP 8642A/B fault messages and diagnostic displays.

Automatic Testing

The HP 8642A/B performs many checks automatically to give the user confidence that it is operating properly. Whenever it is powered on, it executes a 20-second self-test. All display segments are turned on, all 32K bytes of RAM are tested for read/write/addressing, all 256K bytes of ROM have their checksums verified, the EEPROM used for calibration data has checksums and write protection verified, and the 68000 microprocessor is functionally checked. The instrument is set to a variety of frequencies, modulations, and output vernier settings to verify that the loops remain locked. To establish confidence in the fault detection circuitry, each loop is forced to an illegal state that will generate an error signal if the circuitry is working properly. All tests are performed with all attenuator pads in to protect anything that might be connected to the output connector. Finally, the instrument is returned to the preset configuration. For any failures detected during the self-test, appropriate messages are stored to be viewed at the user's convenience. The display flashes to indicate that failure messages are stored. Depending on the SRQ mask, an HP-IB controller may also be interrupted by detection of an error.

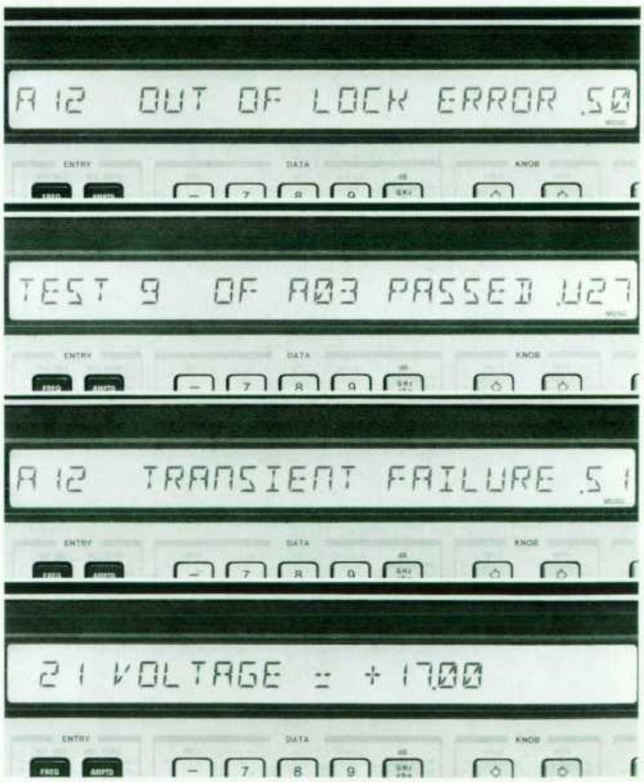


Fig. 1. *Typical HP 8642A/B error messages and diagnostic displays.*

After the turn-on test, circuitry within the HP 8642A/B continuously monitors the phase-locked and ALC loops to trap any errors. The error messages identify whether the specific loop is continuously out of lock (OOL) or had a transient or spurious OOL. The OOL detection circuitry is disabled during switching to avoid misleading messages.

Whenever a user entry occurs, the firmware makes various bounds checks for valid states. Some of the circuits (e.g., the frequency counter) are tested during state changes. When an instrument state is saved, the battery capacity is checked.

Semiautomatic Diagnostic Aids

Similar to the turn-on test is the instrument-level self-diagnostic (ILSD). The ILSD requires three to six minutes to run, depending on model and options. This self-test exercises essentially all of the circuits in the entire instrument. Over 1000 measurements are made at various frequencies, bands, modulation configurations, and amplitude levels. It is an extremely comprehensive functional test of the HP 8642A/B. While impractical to prove, it is estimated that greater than 80% of all functional failures will be detected by this collection of subtests. The HP 8642A/B may also be configured as an HP-IB system controller so that an external printer produces a hard copy of the test results. The test may be run in an infinite loop for intermittent failure checking. There is also a stop-on-error mode to preserve the instrument state for a detected failure. All of this can be controlled from the front panel without any tools or disassembly. In many cases, this test will identify the specific module to be replaced.

Each of the subtests in either the turn-on test or the ILSD can be run separately. There are additional semiautomatic diagnostics that require an operator to move some cables. All of these individual diagnostics are useful either for verifying a failure or for tracing a fault to the component level. All of them may also produce hard-copy results, infinitely loop, and stop on errors like the ILSD.

The turn-on RAM test checks all 32K bytes by reading, inverting, reading, inverting, and reading. This test is nondestructive and will catch most failures in RAMs that were previously tested good in the factory. The ILSD contains a more comprehensive RAM diagnostic that conducts a walking-ones test. After testing, each RAM section's swapped-out contents are restored. In both tests, if an error is found, the failed RAM chip is identified.

There are various tests to manipulate the display in several ways for checking groups or individual character segments and annunciators. Another test prompts the operator to press the keys in a certain order and records any errors.

For the modulation section, one of the semiautomatic diagnostics prompts the operator to connect the unsensed modulation output to the external AM and FM inputs. The built-in routines then manipulate the instrument hardware such that the existing peak detector can be used to check the level out, the audio frequency, and the integrity of the input/output paths.

In the reference summation loop, the built-in diagnostics check several aspects. First, the integrity of the OOL detection circuitry must be verified. Each loop may be put into an illegal state that should always generate an OOL signal. For many, this is accomplished by turning off one of the RF input signals to the loop. The absence of a reference should make any properly working phase-locked loop generate an OOL signal. A message is generated if this does not happen. Once the OOL detection circuitry is known to work, the diagnostics will set the instrument to frequencies that require the particular loop under test to lock at the high, middle, and low points of every oscillator band. Lock acquisition time and power output are checked for each point. Loop lock is also tested with worst-case legal FM modulation on. Both transient and steady-state failures are recorded.

In the output section, because of circuit-to-circuit variations in overrange capabilities, some of the diagnostics are adaptive. The algorithm first checks for actual capability above a specified limit, then uses the result for overmodulation testing.

Component-Level Manual Aids

Experience with previous instruments has demonstrated the usefulness of having convenient access to interesting circuit points. The shielding requirements of an instrument such as the HP 8642A/B prohibit the indiscriminate addition of connections through the casting walls. Therefore, only one return line is allocated to each module. This line is multiplexed inside the module with several useful circuit nodes and the OOL detection line. The service feedback lines go to the I/O board and are connected in parallel to the OOL latches and an analog multiplexer which selects one line for the voltmeter (Fig. 2).

The internal dc voltmeter consists of a comparator and a 10-bit DAC, which perform a successive approximation under firmware control. A precision voltage reference and ground are measured before the selected point to calibrate the reading. Since some of the sense points are prescaled before being multiplexed, the firmware performs postscaling before displaying the reading.

If a more accurate measurement, an ac reading, or an oscilloscope display of a waveform is required, there is a buffered test point on the I/O board where external equipment may be connected to the built-in multiplexer network. This eliminates much unnecessary mechanical disassembly during troubleshooting and allows for RF circuit observation *in situ*.

There is also an uncommitted input to the multiplexer network on the I/O board. A user can connect a clip lead to this test point to measure arbitrary circuit nodes. This capability often eliminates the need for additional test equipment.

One of the voltmeter's multiplexer inputs has an RF detector with response to approximately 1 GHz, along with a coaxial cable. When this point is selected, measured power is displayed in units of dBm. While not accurate enough for calibrating the HP 8642A/B, it is sufficient for troubleshooting the internal RF paths.

Once a problem has been isolated to a relatively small circuit, the technician may need to exercise this circuit in specific ways. Selecting a high-level instrument state (e.g., frequency, amplitude, etc.) corresponding to the desired circuit state requires very detailed knowledge of the instrument. In the HP 8642A/B, there are many service functions that allow control at many levels. For instance, the fre-

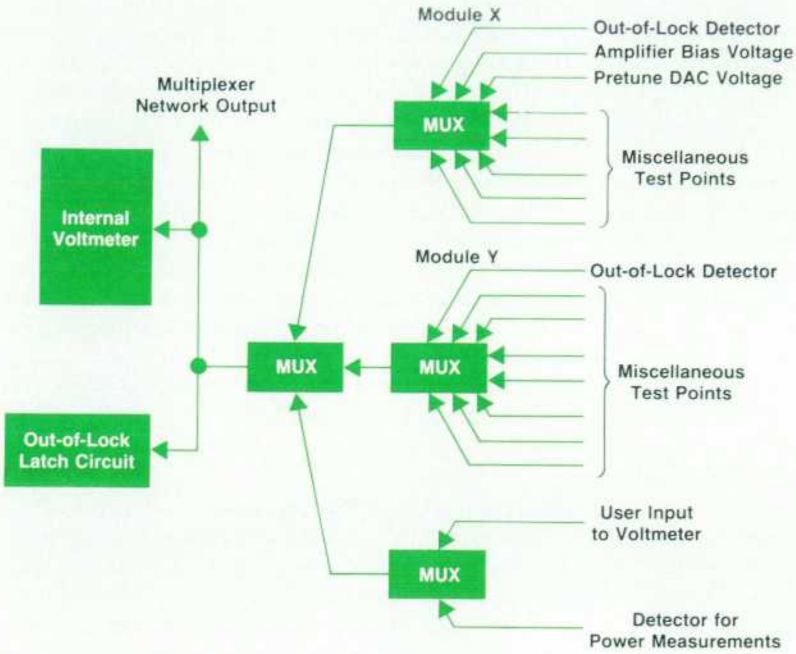


Fig. 2. *To minimize connections through casting walls, only one service feedback line is allocated to each module. These lines are connected in parallel to the out-of-lock latches and an analog multiplexer, which selects one line for the voltmeter.*

quency counter may be used in all of its modes with simple commands, or the user may set and clear each of the counter's control bits individually. There are intermediate levels of user control for other sections. All control bits, DACs, and serial data receivers can be individually configured. It is often useful to know what state a bit should be in, and compare this to the actual state. Service functions exist that return supposed bit states, latch contents, and loop output frequencies.

All of these service functions are available over the HP-IB as well as locally.

Signature Analysis for Computer Core

The diagnostic aids previously discussed depend on the internal microcomputer's working to a minimal extent. This, of course, may not always be the case. For component level repair of the digital control circuitry, extensive digital signature analysis is designed into the HP 8642A/B. Jumpers are used to open the data path from the microprocessor to force a free-run condition for testing the 68000, addressing logic, ROM contents, and miscellaneous logic. Next, interrupt operation can be verified by use of a switch that causes a continuous request. There are two signature analysis routines in the ROM for additional testing. One is a RAM test, which does not use any stack or variables itself. The routine exercises the RAM by writing patterns into it and reading them back out. In addition to the normal extender boards for the microprocessor and I/O boards, there is a special signature analysis board for the I/O board. The I/O board's outputs are rerouted to its inputs, and the second signature analysis routine exercises the input and output latches with specific patterns.

Assurance of Calibration

For situations where the HP 8642A/B specifications must be verified, a trip to the standards lab may be eliminated by use of an HP 8952S Signal Generator Test System. This system is compact enough to be taken to the systems in which HP 8642A/Bs are installed. Calibration can be verified without removing the HP 8642A/B from the rack. Since this verification takes less than an hour, system downtime can be minimized.

On-Site Calibration after Module Swap

It is common for programmable instruments such as the HP 8642A/B to be installed in large, multibay test systems. The cost of such systems often necessitates their continuous operation. In many cases, the support costs of these systems may far exceed their original costs, so the minimization of downtime has extremely high priority. In the past, the MTTR (mean time to repair) of a complex instrument usually was quite long. Often the most reasonable choice was to stock extras of each instrument and to swap the entire box.

With the HP 8642A/B, an on-site service strategy can be employed instead. Using an on-site service kit, a trained technician can isolate the problem to a module, replace the module, and recalibrate the instrument in no more than two hours for most failures (not counting travel time). This on-site strategy uses the ILSD, other built-in diagnostic routines, and the internal voltmeter. Once a module has been replaced, the loading of its calibration data takes only minutes (see box, next page). The bad module can be exchanged and component repair performed off-site as convenient. The transfer of calibration data used in this strategy effectively decouples the problems of keeping production systems running and servicing instruments. Repair and calibration facilities can operate in an orderly and efficient manner with a minimum of fire-fighting.

Self-Calibration of Individual Modules

After component-level repair of a module, it is to be expected that the previous calibration data is no longer valid. The major goals in obtaining new calibration data are (in order of importance): reliability, minimum set of required equipment, minimum operator training, and minimum operator time. With these goals in mind, the capabilities of the internal computer are exploited. Automatic calibration routines are built into the HP 8642A/B for obtaining the needed data for repaired modules.

These routines have extensive checking built-in to reduce the accidental occurrence of wrong setups or incorrect test equipment. An HP-IB printer can be used to obtain a hard copy of the generated data. Once these routines are executing, the only operator requirement is for an occasional setup change. The operator is free to attend to other tasks for most of the calibration time. The worst-case equipment requirements for any of these routines are quite modest. Depending on the routine selected, an HP 8901A or HP 8901B Modulation Analyzer or an HP 8902A Measuring Receiver may be needed. Some of the routines require a system DVM that is HP-IB compatible and performs dc and ac voltage measurements. The command set of the DVM is not critical. Miscellaneous cables and adapters are required and are provided in the bench service kit. A printer is always optional. No other equipment is required for any of the self-calibration routines.

The reference summation loop is a good example of this built-in self-calibration. For each setup, the HP 8642A/B first verifies: 1) that the proper internal connections have been made, 2) that the proper connections between the HP 8642A/B and the external test equipment exist, and 3) that the proper external test equipment is on the HP-IB and is correctly configured for the particular set of measurements. Next, the HP 8642A/B hardware is tested to check that it is functioning properly and has the required adjustment ranges. Various loops have multiple oscillator bands, each of which must be separately calibrated. Each band's tuning curve is characterized first. Hundreds of voltage and frequency measurements are required for this and are automatically taken. There is a shaper circuit that corrects the oscillator sensitivity to the desired value. This shaper circuit must also be characterized. For each of the hundreds of calibration points, the pretune and shaper corrections must be individually calculated. This data is then automatically stored in an EEPROM (see box on the right).

Similiar routines exist for the modulation section, the FM loop, the heterodyne module, and the output section. Some of the modules in the HP 8642A/B do not require such calibration.

External Automatic Calibration

The built-in self-calibration does not answer the calibration needs of all situations. There may be occasions where a different set of test equipment is to be used, occasions where a different weighting exists for the calibration goals listed above. For these and other cases, the HP 8642A/B can have its calibration data entered in another way. All of the data can be entered and read out over the HP-IB by any bus controller. With the multiple levels of control available through service functions, the circuitry can be manipulated in the same manner as by the self-calibration routines.

Acknowledgments

I would like to acknowledge the help of Rodger Tracy and Jon Sigler in educating me to our customers' needs and in developing this support strategy. Chris Farnes deserves much credit for his day-to-day help and suggestions, as well as for the comprehensive and professional job he did on the support documentation. Morris Chase and Jerry Richardson performed much of the testing and critique of the procedures, hardware, firmware, and documentation. Chuck Kogler implemented a considerable share of the support firmware. None of this could have happened without the significant managerial support of Art Upham. I would also like to thank the other members of the R&D team for their cooperation and help where their hardware/firmware was concerned.

Electrically Erasable PROM Storage for Calibration Data

With the HP 8642A/B's extensive use of software calibration, it was necessary to find a better way of storing calibration data than had been used in previous instruments. The requirements were reliability, ruggedness, low cost, and convenience. These criteria eliminated such alternatives as battery-backed-up RAM, normal EPROMs, bubble memory, disc, and tape storage. It was felt, for example, that if calibration data for the attenuator needed to be replaced, a technician should not have to remove the microprocessor board. Indeed, it is strongly desirable to be able to store such data over the HP-IB.

The choice made for the HP 8642A/B was to use five-volt-only EEPROMs. These parts have data retention times equivalent to normal EPROMs. The write cycles are specified in the tens of thousands, which is orders of magnitude beyond any conceivable number of recalibrations in one instrument's lifetime. These EEPROMs are soldered directly into the microprocessor board, without sockets. This provides great ruggedness and reliability. In normal operation, the EEPROMs are write-protected by a physical switch, which is conveniently located on a tab on the top of the microprocessor board.

On-site support has additional requirements. When a module is swapped to repair an HP 8642A/B, it is accompanied by a small printed circuit board (calboard) with a pair of EEPROMs on it. These are mapped like the pair on the microprocessor board, but they contain only the calibration data for the new module. The person repairing the HP 8642A/B on-site uses a service function to transfer the new data from the calboard to the microprocessor board. A new snapshot of the entire instrument's data is put into the calboard as a backup. The calboard resides in a box on the rear panel of the HP 8642A/B, to be used in case the microprocessor board requires replacement.

Various service functions exist for examining valid data in both resident EEPROM and the calboard, comparing the contents of the two, and performing a variety of data transfers. Each module's calibration data has its own checksums. Substantial effort was expended in making the handling of calibration data forgiving and safe. Appropriate messages are generated for cases of unprotected and invalid data.

In addition to calibration correction data, several other types of information are stored in the EEPROM. Included are instrument model number, serial number, list of installed options, calibration methods used for each module, data of last calibration, and version codes for the modules.

Internally Modular Signal Generator Mechanical Design

by Michael B. Jewell and Mark W. Johnson

ONE of the principal goals for the mechanical design of the HP 8642A/B Signal Generator was to provide effective shielding to ensure high performance without sacrificing serviceability or ease of manufacture. This ruled out "stiff" RF gaskets, large numbers of screws, retaining nuts for RF connectors, and covers that can't be removed without unsoldering components.

The design that realizes these goals divides the circuitry into functional blocks or modules. These modules are treated as small, complete instruments that have well-defined input and output specifications, require minimum external inputs (power, digital control, and RF signals), and can be completely built and tested before final assembly, which then requires a minimum of testing and adjustments for the assembled instruments to meet specifications.

The module design is illustrated in Fig. 1. Each consists of two printed circuit boards sandwiched between three die castings for shielding. The printed circuit boards have ground planes on both sides extending to the edges and between all sections that need shielding from each other. Through these areas are many closely spaced plated holes connecting the two sides of the board, thereby effectively forming a continuous ground plane, which prevents RF energy in the board material from escaping. These ground plane areas are also the places where the cast base and cast covers make electrical contact through the main RF gasket material.

All RF connectors and power or control feedthrough fil-

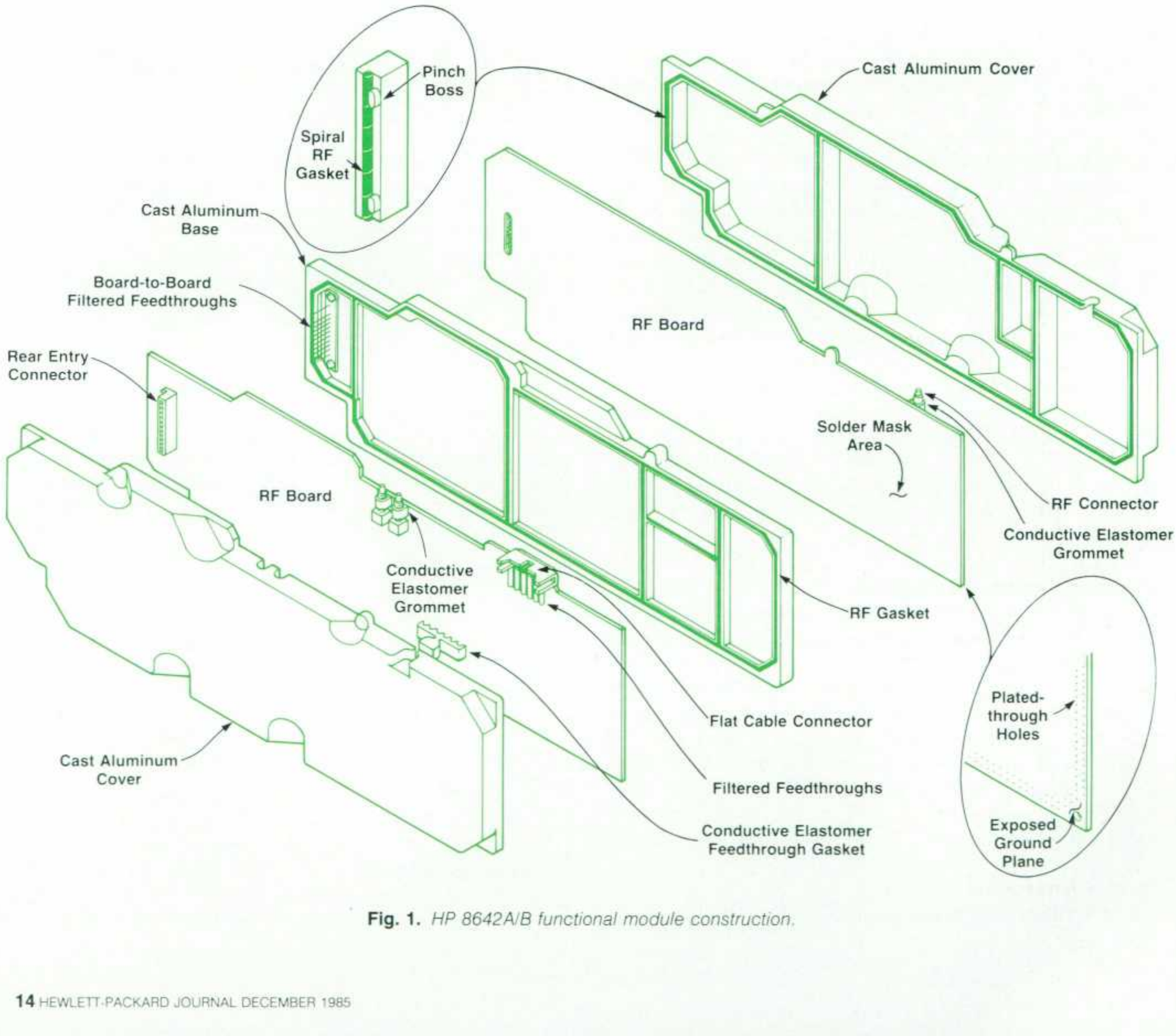


Fig. 1. *HP 8642A/B functional module construction.*

ters that must pass through the shielding are grounded immediately at the shield by conductive elastomer grommets. This ensures that a good ground connection is made immediately at the shield, which is optimum for keeping RF noise on a wire or cable outer conductor from radiating inside the shielded enclosure. Yet, when the screws that hold the cover on are removed, there are no additional nuts, solder joints, or other connections preventing removal of the cover, and all electrical components are intact and functional, allowing operation of the circuitry for troubleshooting.

Power and control lines come to a module over a flat cable from a power and digital distribution board (Fig. 2). This cable attaches to one of the boards in the module. Printed circuit traces then lead to the filter feedthroughs mentioned above. Power and digital signals are delivered from this board to the other board in the module through feedthrough filters, which are attached to the base casting and plug into rear-entry connectors on each board.

The main RF gaskets are spiral-wound metal strips, which are attached to the castings by being pinched periodically between a low wall and short bosses as shown in Fig. 1. Because the gaskets are soft and the castings are stiff, few screws are needed to hold the covers on, thereby greatly improving serviceability.

The sandwich design provides for a continuous ground connection, which completely surrounds each shielded section of circuitry—above, below, and through the printed circuit board. Compared to the older, more common practice of grounding boards at a few discrete locations, this technique provides much more predictable RF performance and much higher levels of shielding.

The custom die castings allow internal and external walls to be placed virtually anywhere, making possible a large number of shielded compartments on a single printed circuit board.

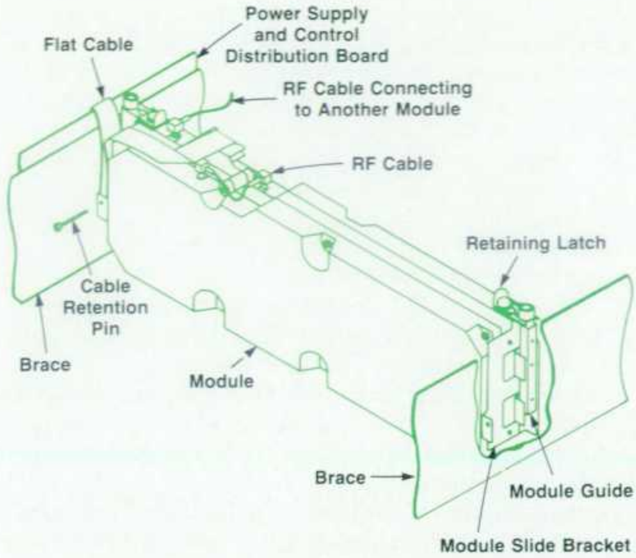


Fig. 2. *Power and control lines come to a module over a flat cable. Sliding snap fasteners secure each module to guides attached to the frame.*

Thermal Considerations

The thermal conductivity of the aluminum castings tends to provide very uniform temperatures inside the modules even when power is concentrated in certain areas. In addition, the number and location of air holes can be tailored

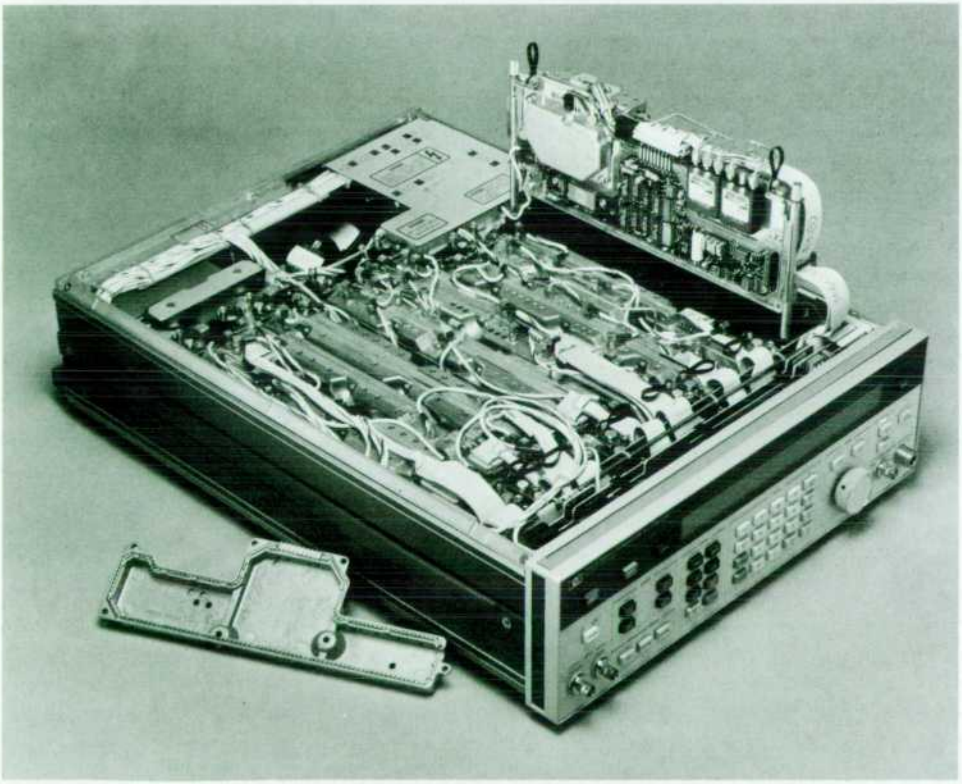


Fig. 3. *Module pulled out and covers removed for service.*

to the power being dissipated in each module.

Cooling is accomplished by drawing air up through the modules first, then through the high-performance, dc ball-bearing fan, across the power supply rectifiers, and lastly through a heat sink holding the power transistors.

The fan is centrally located in the air flow path and is totally enclosed in the instrument, which greatly reduces the external noise level.

Serviceability Considerations

The modules are mounted in the instrument as shown in Fig. 2. Two sliding snap fasteners secure each module to guides attached to the internal framework.

A four-color silkscreened diagram on the inside of the instrument top cover provides a detailed map for servicing. An RF connector wrench and fuse puller are mounted inside the instrument.

To replace a module, the two snap fasteners are disconnected, cables are removed, and the module is lifted out and replaced with a known good module. For operating module repair, extender pins are screwed into the tops of the two guides mentioned above. The snap fasteners are then unlatched, the module is pulled up, and the snap fasteners are reconnected at the top of the extenders. The covers can now be removed and the printed circuit boards examined while fully powered-up (see Fig. 3).

Advantages of the Design

Because of the conductive elastomer grommets used to ground the connectors and feedthroughs and the use of a soft RF gasket, access to HP 8642A/B printed circuit boards is obtained by removing only a small number of screws. This provides high serviceability while maintaining very high shielding levels.

The modularity concept, with its fully specified and tested modules, provides high manufacturability and serviceability. Manufacturability is high since each module's performance specifications are verified as a separate unit, so that when the modules are assembled into the instrument, the entire instrument will have a very high likelihood of meeting overall performance specifications. Serviceability is high since modules can be swapped in an instrument in the field and the instrument will still meet its performance specifications.

Liquid Crystal Display Backlighting

Because of the serviceability and ease of use goals for the HP 8642A/B, it was decided that a large alphanumeric display would be required. At the same time, low power consumption and low EMI were important. A liquid-crystal display (LCD) fit all of the requirements. One drawback with LCDs, however, is that they are not readable in the dark. The design team considered this condition unacceptable (even though it often exists) and designed a method of backlighting the display.

Some of the goals for the design were:

- Bright, uniform lighting of a very long LCD
- Highly reliable light source
- Ability to fit in the minimal space behind the LCD.

The construction and operation are best explained by describing each of the parts individually. The letter designations for parts refer to Fig. 4.

The LCD printed circuit board (a) is designed with the driving circuitry surface mounted on the back side. This provides the maximum space available for the backlight and minimizes the number of external interconnections.

The main reflector (b) is a brilliant white plastic sheet that lies along the frosted (roughened) back surface of the backlight and wraps around the light bulbs and parabolic sections at each end. Its function is to reflect and diffuse back into the backlight any light that leaves from the back surface. It is important that this be a separate part, not in intimate contact with the backlight, to preserve the total

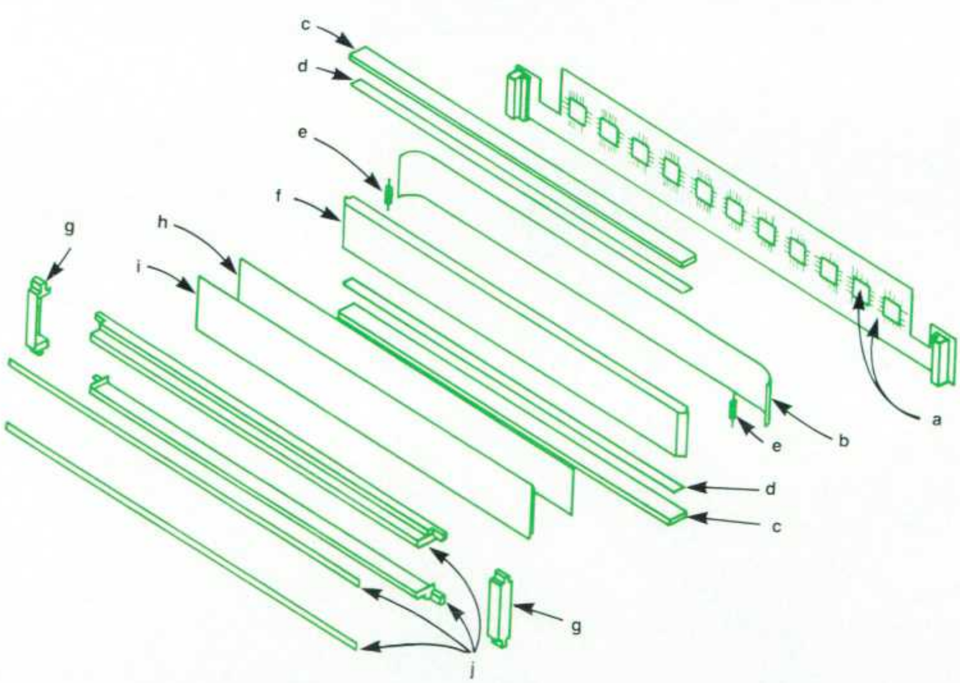


Fig. 4. *LCD display construction. (a) LCD printed circuit board. (b) Main reflector. (c) Conductive elastomer connectors. (d) Spacers/reflectors. (e) Light bulbs. (f) Backlight. (g) Locators. (h) Diffuser. (i) LCD. (j) Retaining hardware.*

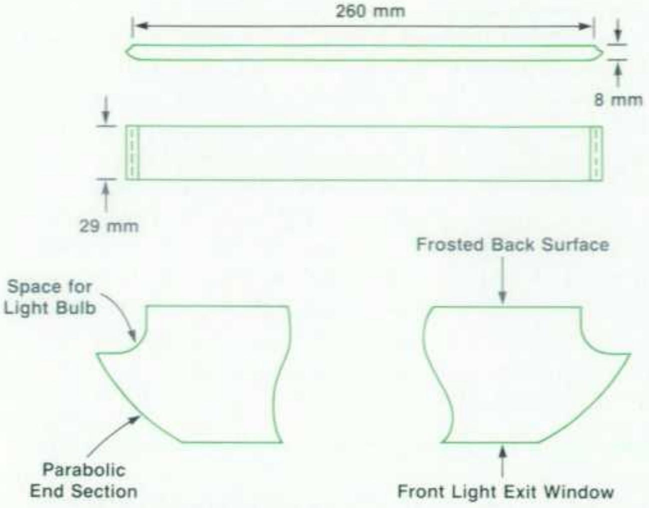


Fig. 5. *Backlight detail.*

internal reflection (TIR), which predominates at the back surface of the part. Aluminizing or white paint on the back surface would not work here, since these substances have a high index of refraction. This could eliminate or reduce the possibility of TIR since this phenomenon depends on light traveling in a medium with a high index of refraction compared to the surrounding medium.

The conductive elastomer connectors (c) have many parallel rows of conductive rubber separated by nonconductive rubber. They connect a conductor on the LCD board to contacts on the backside of the LCD.

The white spacers/reflectors (d) keep the elastomer connectors from coming into intimate contact with the light bar. This also preserves TIR. The light sources (e) are axial-leaded incandescent bulbs.

The backlight (f) is a molded clear acrylic part which takes light from the lamp at each end and distributes it uniformly across the front exit window (Fig. 5). The frosted back side produces a mostly diffuse light source whose intensity is not strongly affected by viewing angle. The light leaving the lamp is largely collimated by the cylindrical approximation of a parabolic reflector at each end. It then travels down the backlight and is eventually intercepted by the frosted back surface of the part. Here it is reflected and diffused and exits through the front of the part. To compensate for greater absorption and internal reflection toward the center of the part than at the ends, the roughness of the back surface is nonuniform, being greater toward the center than at the ends. By tailoring the surface roughness, the intensity of the exit light can be made extremely uniform over the entire length of the part.

Two locators (g in Fig. 4) position the backlight and light bulbs while holding the main reflector in contact with parabolic ends of the backlight.

The diffuser (h) is a thin sheet of frosted clear plastic, which takes the already mostly diffuse light exiting the backlight and further diffuses it, producing a light source that is even more uniform and has unnoticable dependence on viewing angle. The LCD (i) is a standard wide-temperature-range transmittive LCD.

Advantages

The unit operates with only two bulbs driven at a level that guarantees very long bulb life. If one light should burn out, the illumination drops noticeably, but is still very usable and very uniform. This allows the user to continue

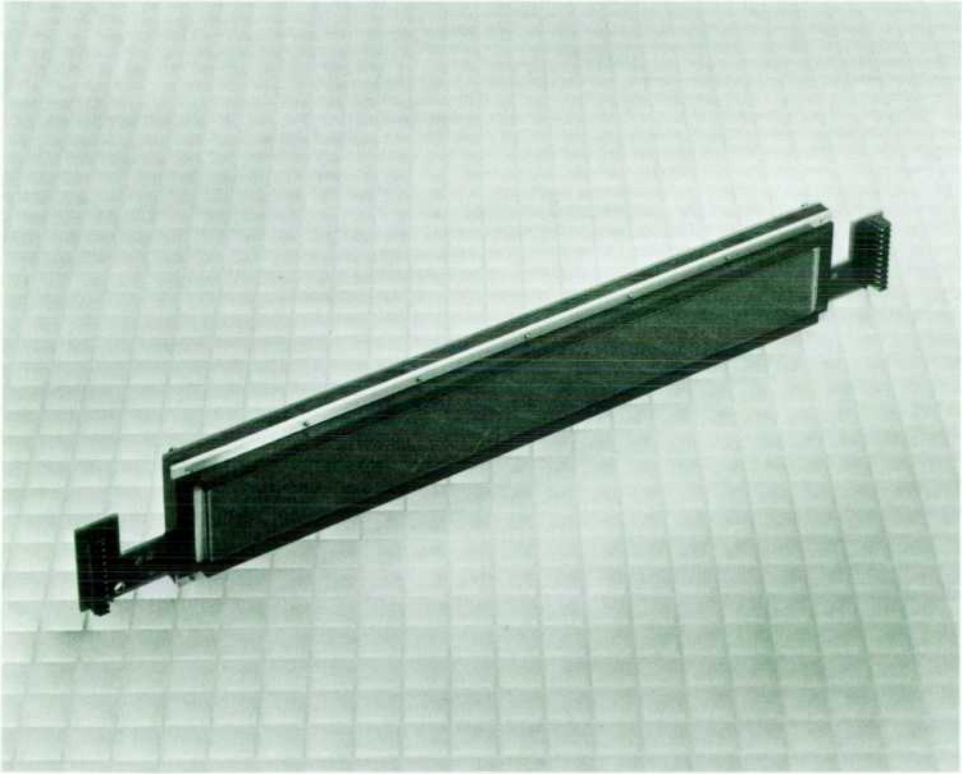


Fig. 6. *LCD module.*

to use the display in a dark environment while scheduling maintenance to replace the bulb. The backlight provides bright, uniform illumination for a very long LCD in the minimum thickness behind the front panel normally needed for standard switches. From service and manufacturing standpoints, the finished, fully tested LCD assembly (Fig. 6) is just another module, which can very easily be swapped, both in the field and on the assembly line.

Acknowledgments

Patty Decker-Morton worked on shielding and early attenuator concepts. Pat Herron and Bruce Roeder worked on attenuators. Lee Olmstead contributed greatly to the LCD backlight. Billy Reynolds was invaluable as manufacturing and production engineer. Gene Mertz and others in components engineering were a constant resource.

Many people on the assembly line, in printed circuit board design, quality assurance, the fab and model shop, drafting, lab services, purchasing, and elsewhere in the company contributed ideas, refinements, and energy.

Wide-Frequency-Range Signal Generator Output Section Design

by Robert R. Collison, James B. Summers, Marvin W. Wagner, and Bryan D. Ratliff

TWO OUTPUT SECTIONS are used in the HP 8642A/B Signal Generator to cover the 0.1-to-1057.5-MHz frequency range. In the HP 8642B, a doubler output section is added to cover the 1057.5-MHz-to-2115-MHz frequency range.

Fig. 1 is a block diagram of the two output sections—the UHF output section and the heterodyne output section. Fig. 2 is a block diagram of the doubler, attenuator, and reverse power protection section. Both the UHF and the doubler output sections contain power-amplifier/peak-detector microcircuits and ALC loops. While similar in some respects, these elements are not the same in the two sections and are discussed separately in this article.

The range of 4.1 MHz to 1057.5 MHz is generated by dividing the main octave of 528.75 MHz to 1057.5 MHz with binary dividers (divide by N, where N = 1, 2, 4, 8, 16, 32, 64, or 128).

To obtain frequencies from 0.1 MHz to 4.1 MHz, the heterodyne output section is used. The heterodyne LO is a 45-MHz reference signal that originates in the HP 8642A/B time base, and the RF signal is a 45.1-MHz-to-49.1-MHz signal from the output of the UHF output section (the ÷16 band). This selection of heterodyne input frequencies maintains good carrier noise performance and uses a convenient, available LO frequency.

To generate wide-deviation FM with low distortion from 0.1 MHz to 131 MHz (particularly useful for the home entertainment market in the 88-MHz-to-108-MHz range and for characterizing IF amplifiers), the same heterodyne output section is used, but with higher RF and LO frequencies. Normally, this frequency range is covered by the main octave divided by N via the UHF output section. Choosing to divide by N provides the best carrier noise performance, but also divides the amount of FM deviation from the main octave by N. Therefore, N times the amount of FM deviation is required in the main octave, which increases FM distortion. By using this heterodyne band, the amount of FM deviation required from the main octave is reduced. This reduces FM distortion for a given FM deviation and increases FM deviation capability for this frequency range. This benefit is offset by higher carrier noise, which is usually not a concern when using large FM deviations. The heterodyne LO for this range is an 832.5-MHz SAWR (surface-acoustic-wave-resonator) reference oscillator locked to the 45-MHz reference, and the RF input signal is an 832.5-MHz-to-963.5-MHz signal from the UHF output section.

The UHF and doubler output sections have ALC loops to control the output vernier power level and generate the desired AM. In the heterodyne bands, these functions are done by controlling the RF input signal to the heterodyne output section from the UHF output section, since the heterodyne section has no ALC loop. This allows amplitude modulation at low RF frequencies and simplifies ALC bandwidth switching.

Critical Design Issues

The critical requirements for the output sections were high output power capability with low RF harmonic distortion, low output intermodulation distortion, low incidental AM and PM, accurate wide-bandwidth AM with low AM distortion, low residual AM and FM, low noise contribution, good RF output impedance, accurate RF output level to very low levels, and reverse power protection. Features added for increased flexibility include amplitude sweep, ALC off, and attenuator range hold. Digitally stored calibration is used to correct output RF level and AM level to increase accuracy.

One of the prime applications for the HP 8642A/B is as a stimulus for testing very sensitive receivers and pagers.

Typically, testing of these receivers includes sensitivity characterization (typically on the order of 0.2 μV) and SINAD measurements. To do this characterization accurately, the stimulus must have very good output level accuracy down to very low levels, and at the same time, must maintain low RF leakage to prevent stimulation of the receiver by radiation. The HP 8642A/B maintains an output level accuracy of ± 1 dB down to -127 dBm (0.1 μV), which is adequate to test most receivers. From -127 dBm to -140 dBm (0.022 μV) the accuracy is ± 3 dB. Low leakage is maintained by shielding techniques, which are a part of the HP 8642A/B module concept. Also, proper dressing of cables and RF leakage tests of assembled instruments ensure low leakage.

UHF Output Section

The UHF output section takes the unleveled, harmonic-rich output from the dividers of the sum loop and converts it into a leveled sinusoidal output. Amplitude and pulse modulation and amplitude sweep are also accomplished in this module.

The block diagram of the UHF output section is shown in Fig. 1. The RF signal from the dividers ranges in frequency from 4.1 to 1057.5 MHz, and in level from 0 to 6 dBm. As this signal enters the UHF output module, its level is amplified to +15 dBm by an amplifier whose last stage is driven into compression. The output of this amplifier, ranging between +15 and +17 dBm, drives an amplitude modulator.

The amplitude modulator is a switching type modulator that acts as a programmable limiter. Since its input signal is rich in harmonics anyway, no penalty is paid because of harmonic generation. In fact, any even-order harmonic components in the modulator input signal that are caused by asymmetries (other than duty cycle) are suppressed. The main benefit of this modulator configuration is that its output signal level is not a function of its input level as long as the input level is above a limiting threshold level. This prevents variations in the divider output level from affecting ALC bandwidth. The switching modulator also exhibits a better noise floor than a pin diode modulator.

The output of the amplitude modulator is applied to the low-pass filter section. The signal is buffered and sent through one of sixteen low-pass filters. The corner frequencies of these filters are spaced every half octave to guarantee that the second harmonic of the lowest frequency used

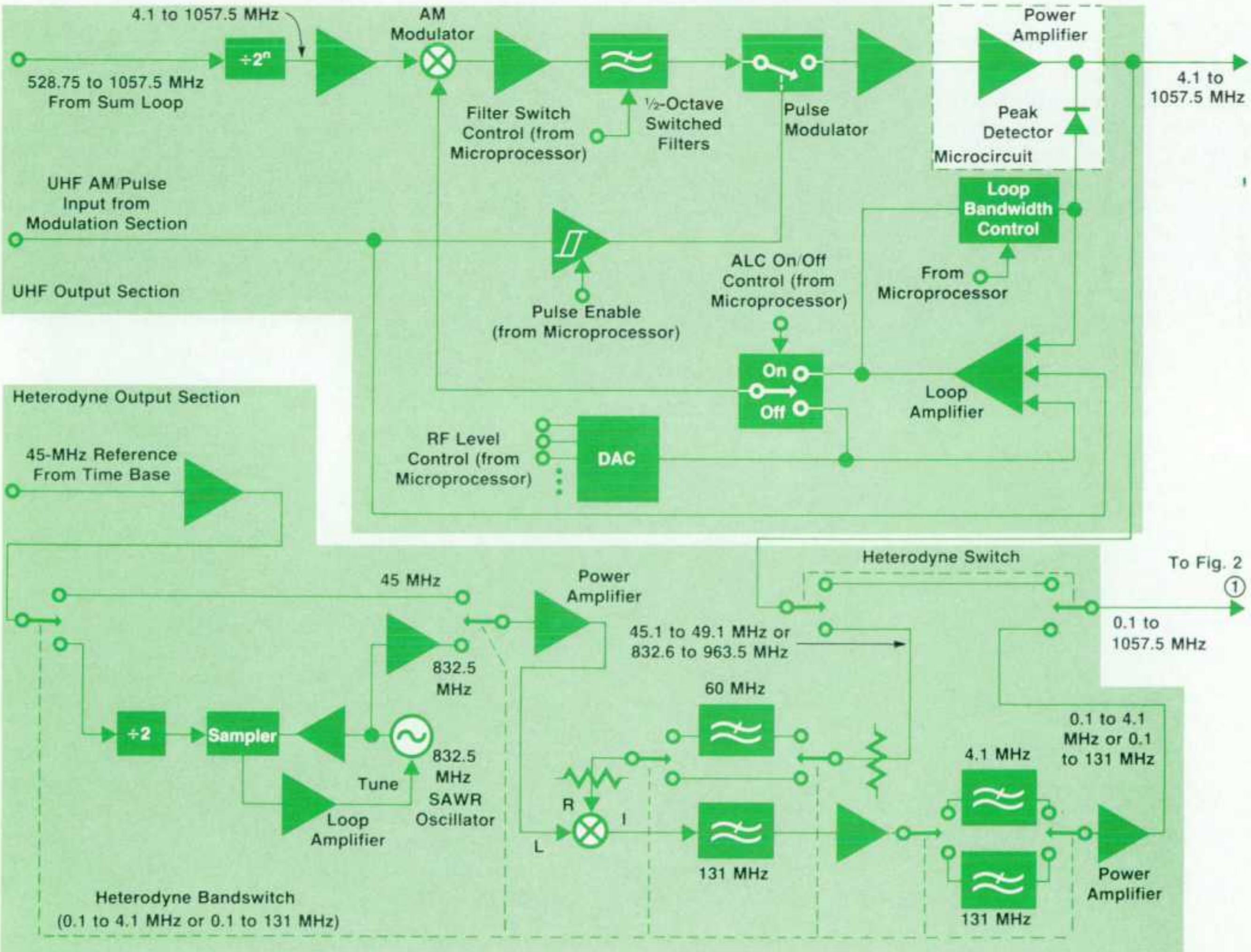


Fig. 1. *HP 8642A/B Signal Generator UHF and heterodyne output sections.*

with a particular filter is at least one half octave above the cutoff frequency of the filter. The filters are arranged in two banks of eight filters each to ease the requirements on the pin diodes used as the switch elements.

Once through the filters, the signal passes through a pin diode switch, which is used for pulse modulation. The pulse modulator is placed after the filters to avoid ringing, which would otherwise occur as the filters attenuated some of the spectral components of the pulse modulated signal.

The output of the pulse modulator is amplified to the levels required to drive the output power amplifier. The output power amplifier is a thick-film microcircuit that contains a pair of microwave bipolar transistors connected in a Darlington configuration. The use of series and shunt feedback produces a flat gain response as well as a low output impedance at the collectors of the transistors. The output amplifier microcircuit also contains the ALC peak detector and the backmatch resistor. The low output impedance of the amplifier keeps the ALC loop bandwidth from changing as the load on the amplifier is varied. In conjunction with the backmatch resistor, the low output impedance provides a broadband match.

The peak detector on the power amplifier microcircuit senses the amplitude of the output signal. In the loop amplifier, the peak detector signal is compared with signals from the level vernier DAC (digital-to-analog converter) and the AM input from the modulation section of the instrument. The output of the loop amplifier drives the amplitude modulator to force the detector output signal to equal the sum of the vernier DAC and AM signals, thus performing the automatic level control function.

The frequency response of the loop amplifier determines the bandwidth of the ALC loop. When no AM is required, the ALC loop bandwidth is reduced to 200 Hz to provide the best noise and intermodulation performance. When AM is desired, the ALC loop bandwidth is widened to provide 100-kHz AM bandwidths for carrier frequencies greater than 33 MHz, and 20-kHz bandwidths for carrier frequencies less than 33 MHz. At 33 MHz, the detector response is altered to prevent ripple on the detector output from causing amplitude errors at the lower frequencies. Thus it cannot respond to AM envelopes as fast as it can at higher frequencies, so the bandwidth is restricted.

An ALC OFF mode allows the vernier DAC to drive the modulator directly. In this mode the ALC loop is opened and level accuracy is determined by stored calibration data. ALC OFF mode is used for the best intermodulation performance at small offsets, as well as in pulse mode. In pulse mode, using the open-loop configuration eliminates the need for a minimum pulse repetition rate.

Design for Low Noise

One of the primary design goals for the UHF output section was that it contribute little to the overall instrument noise. There are two mechanisms by which the UHF output section can affect the noise level of the signals passing through it.

Multiplicative noise is noise modulated onto the RF carrier primarily by the amplitude modulator. This is almost entirely amplitude noise (in phase with the carrier), since the modulator has been designed to minimize incidental phase modulation. To minimize multiplicative noise, emphasis was placed on low-noise design throughout the baseband ALC circuitry. Also, the level vernier DAC and

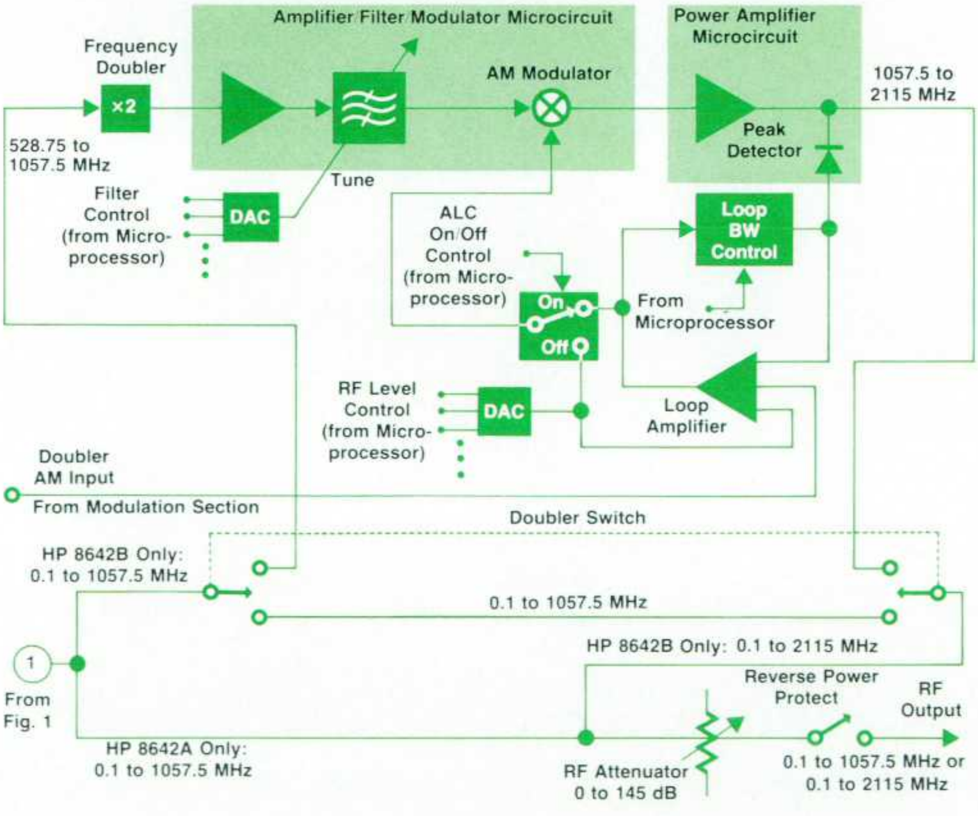


Fig. 2. *HP 8642A/B doubler output section (B model only), output attenuator, and reverse power protection.*

AM signals are summed separately into the ALC integrator. This allows noise from the high-impedance DAC circuitry to be filtered without affecting AM frequency response.

The second noise contribution is additive noise, which results when a signal passes through any stage that contains a noise source. Noise of random phase is added to the RF signal. This noise can be broken into components in phase with the carrier (amplitude noise) and in quadrature with the carrier (phase noise). Additive noise has been minimized by maintaining high RF signal levels throughout the signal path, and by using low-noise stages for amplification and modulation.

The switching modulator offers definite advantages for low-noise operation. First, because its nature is that of a switch, diode current is either zero or twice the signal current for most of the RF cycle. The shot noise contribution of a diode in series with the signal path is inversely proportional to the square root of the diode current when the diode is biased on. The switching modulator exhibits much higher diode currents when forward-biased than does a pin diode modulator. The second advantage of the switching modulator stems from its limiting nature. Amplitude noise from the divider circuitry is reduced by the limiting action of the modulator, typically by about 10 dB.

Output Power Spike Elimination

In the design of the UHF output section hardware and the related processor control firmware, emphasis was placed on the elimination of output power spikes caused by a loss of signal to the ALC loop during divider or oscillator band changes. When the RF signal drops out, the ALC loop attempts to compensate by increasing the control current to the modulator. When the RF signal reappears, the modulator current may be much too high, causing a momentary high power output from the output power amplifier. To prevent this, during band changes the vernier DAC is set to zero and a built-in offset within the DAC prevents the ALC integrator from slewing the modulator current towards full on.

Another potential cause of signal loss in the ALC loop occurs when low-pass filter switchpoints are crossed. To prevent this, the processor always switches the low-pass filters such that the initial and final frequencies are in the filter passband during the frequency transition. Moving up in frequency, the new higher-cutoff-frequency filter is switched in before anything else happens. Moving down in frequency, the current filter is left in until the frequency transition has occurred, and then the correct filter is switched in.

Calibration and Diagnostics

To take full advantage of the powerful microprocessor that controls the instrument, an analog multiplexer is designed into the UHF section circuitry to monitor key voltage levels. Most mechanical adjustments have been eliminated and replaced by microprocessor-controlled DAC adjustments. All test points necessary for calibration and operational verification are brought out through the multiplexer.

Output level calibration is a two-stage process. First the gain and offset of the vernier DAC are characterized, and then the frequency response of the RF peak detector in the power amplifier is determined. Corrected level accuracy at the output of the UHF output section is typically ±0.1 dB over the 4.1-to-1057.5-MHz frequency range.*

Amplitude modulation depth is calibrated by characterizing the detector diode at 17 frequencies. The detector diode exhibits an offset from its ideal characteristic that is dependent upon stray reactances. This offset is measured and stored as correction data. When setting AM depth, the processor uses this offset data and the level vernier DAC voltage to compute the AM voltage required from the modulation section.

As mentioned earlier, operation in ALC OFF or pulse modes depends on calibration data for level control. Here, the output power as function of the level vernier DAC setting is characterized at 22 frequency points and two levels at each frequency. A double interpolation is used to set any arbitrary level at any arbitrary frequency.

Amplitude Sweep

A useful feature of the HP 8642A/B is amplitude sweep. The output amplitude can be swept over a 0-to-20-dB range either linearly or logarithmically. This allows such measurements as amplifier compression testing, log amplifier testing, and detector linearity testing. Amplitude sweep is done with the ALC loop closed to provide good amplitude accuracy and linearity.

Heterodyne Output Section

The heterodyne output section is designed to frequency translate the RF output signal from the UHF output section by means of a mixer and very linear RF and IF paths. In the process, both AM and FM pass through virtually unchanged. The heterodyne output section uses bipolar transistor amplifiers, LC filters, a doubly balanced mixer, a SAWR oscillator, a FET switch, and pin diode switches. The SAWR oscillator and sampling phase-locked loop used for the LO in the 0.1-to-131-MHz band are very similar to those in the frequency synthesis section (see article, page 24) and are not discussed here. The heterodyne switch uses a ceramic substrate with TO-5 relays similar to the output attenuator (see below); it is used to switch the heterodyne section in or out as desired.

As previously mentioned, two heterodyne bands are implemented in the HP 8642A/B to allow the user to choose between a lower-noise output signal or wider-deviation FM capability. This creates special design challenges, since several circuits have to perform well for two ranges of heterodyne section RF input frequencies that are approximately 800 MHz apart in frequency. In some cases, this requires that two different circuits be used. Switching between these circuits is accomplished using pin diode switches and TTL drive circuitry. In both bands, the overall gain of the heterodyne output section is nominally unity.

There were two major design challenges for this section. The first is the suppression of unwanted (spurious) signals generated during the frequency translation process. The guaranteed specification for these nonharmonically related signals is that they are more than 100 dB below the carrier in the 0.1-to-4.1-MHz band. The second challenge is the preservation of the desirable characteristics of the UHF

*This accuracy excludes errors in the measuring instrument.

output section signal, such as level accuracy, spectral purity, and modulation.

Spurious-Signal Considerations

The two primary mechanisms for the generation of spurious signals in the heterodyne section are mixing products and leakage. Since all the amplifiers in the RF signal path are designed to be extremely linear, the only significant source of undesired mixing products is the mixer. To minimize the level of these spurious signals, a high-level mixer is used and the RF level presented to the mixer is kept relatively low. There is approximately 26 dB of attenuation between the heterodyne section input and the RF port of the mixer. Further attenuation of this signal would seriously degrade its signal-to-noise ratio, so it is important that the mixer have low spurious response.

It is also necessary to include switched low-pass filters in both the RF and IF paths (see Fig. 1). The switched 60-MHz low-pass filter is used in the 0.1-to-4.1-MHz band to reduce the harmonics of the RF signal input to the mixer so that they will not mix with harmonics of the LO signal and create spurious signals that cannot be filtered out later. The switched 4.1-MHz or 131-MHz filters in the IF path are used to filter out mixing products that are higher in frequency than the highest-frequency signal desired from the selected heterodyne band. For the higher-frequency heterodyne band, two five-pole filters are used to achieve the desired rejection. In the lower-frequency heterodyne band, one seven-pole filter is sufficient.

Critical Components

Selection of the pin diodes used to switch the low-pass filters is based upon three important parameters that are all critical to the performance of the circuit. The first important parameter is off capacitance. If the capacitance is too high, spurious signals are able to couple around the filters that are designed to reject them. This is especially true in the IF path, where two filters run parallel and one has a much higher bandwidth than the other. The second important parameter is insertion loss. Since the entire heterodyne section runs open-loop, it is important that the diodes have a very consistent forward resistance from diode to diode. This allows repeatable gain characteristics from module to module. The last important parameter of the pin diodes is low-frequency response. The insertion loss of the diodes has to be flat down to 100 kHz so as not to distort the amplitude modulation and frequency characteristics of signals with sideband frequencies as low as 100 kHz. Selecting diodes that can meet all three of these requirements simultaneously was a real challenge: however, a diode and a design meeting all the requirements were found.

Thermal Considerations

As previously mentioned, the heterodyne section is designed for a nominal gain of unity. Spurious-signal considerations require that the RF input signal to the mixer be severely attenuated. This results in a down-converted signal attenuated by more than 30 dB that must be amplified back to its original level. To meet HP class B environmental specifications, the circuit has to work from 0°C to 50°C with less than 0.2 dB variation in net gain, including mixer conversion loss, pin diode insertion loss, attenuator losses, and amplifier gains, all of which vary with temperature. Compensation for all these factors is achieved with a single two-element series network.

A thermistor in series with a resistor is added to the emitter circuit of one of the three amplifier stages. This thermistor has a negative temperature coefficient; as the temperature increases, its resistance decreases and the net gain of the amplifier increases. This compensates for all of the other temperature effects, which have a net effect of lowering the gain with increasing temperature. By adjusting the nominal resistance of the thermistor and resistor as well as the temperature sensitivity of the thermistor, a net gain variation of less than 0.2 dB over the specified temperature range is achieved.

Doubler Output Section

The primary function of the doubler section is to extend the upper frequency limit of the HP 8642B from 1057.5 MHz to 2115 MHz. Fig. 2 shows the overall doubler block diagram.

The input signal that drives the doubler module comes from the UHF output section. The input signal's level is +16.5 dBm and its frequency is between 528.75 and 1057.5 MHz. The frequency doubler is a full-wave bridge rectifier with four diodes that are contained within a single package. This reduces parasitics and improves diode-to-diode matching, which enhances doubler performance. The bridge is driven by a balun made from coaxial cable and ferrite beads to simulate inductors at the frequency of operation. The output signal from the doubler is at twice the input frequency. In addition to the doubled frequency, there are also $nf_o/2$ subharmonics, where $n = 1,3,4,5...$ and f_o is the desired output frequency. These subharmonics are as high as −15 dBc and must be filtered with a tunable bandpass filter that operates from 1057.5 to 2115 MHz. To overcome the 12 dB of conversion loss in the doubler circuit and to minimize additive noise, a gain stage follows the doubler circuit to maintain a good signal-to-noise ratio.

Amplifier/Filter/Modulator Microcircuit

The signal level in the amplifier/filter/modulator microcircuit is increased by 9 dB by a single-stage GaAs FET amplifier that has a flat gain response.

Since the doubled signal has $nf_o/2$ subharmonics as high as −15 dBc, a tunable bandpass and notch filter that operates over the entire doubler frequency range is used to reject the subharmonics by 35 to 40 dB. Two input lines to the filter control the passband and notch response. The calibration of the filter is critical if the subharmonic performance specification is to be met. The microprocessor controls an eight-bit DAC such that when all the digital inputs are at a logic low level, the filter is centered about 1057.5 MHz. When all digital inputs to the DAC are at a logic high level, the filter is centered about 2115 MHz. When characterizing the filter's response, the DAC is set to 33 known states and the 3-dB bandwidth is determined. The center frequency can be calculated from the 3-dB frequencies of each state so that for a given frequency setting an exact DAC number can be calculated to tune the filter properly. From the 33 known DAC numbers and center frequencies, the remaining states are interpolated. When the frequency setting changes by more than 5 MHz, the microprocessor updates the DAC number to tune the filter to the proper center frequency.

The RF signal amplitude is controlled through the use of a two-section pi-configuration modulator to achieve 0.1-dB output level resolution and to provide amplitude modulation. The control devices are pin diodes whose RF resistance, which depends on the amount of dc bias current, determines the RF attenuation. The dynamic range of the modulator is 40 dB. Harmonics on the output of the amplitude modulator are less than −40 dBc, while subharmonics are less than −55 dBc. With the modulator set for minimum insertion loss, its nominal RF output level is +2 dBm.

Power Amplifer and Peak Detector Microcircuit

The power amplifier, which follows the amplifier/filter/modulator microcircuit, provides the necessary output power to meet the RF power specification for the instrument.

The input signal received from the amplifier/filter/modulator microcircuit must be increased in signal level to provide the necessary output power. This is accomplished through the use of a two-stage GaAs FET amplifier which uses feedback to maintain a flat gain response. The first stage has a drain voltage of +5V and a drain current of 220 mA. The second state has a +7V regulator and a drain current of 230 mA. The overall gain provided by the output amplifier is +18 dB.

The RF peak detector, which is also located in this assembly, is used to sense the RF level on the drain of the output stage. The detector uses two diodes in series, which reduces the junction capacitance to provide the desired frequency response and increases the breakdown voltage capabilities to meet the RF power requirements. A temperature compensation circuit, containing two diodes similar to the detector diodes, cancels the effects of the detector diodes' junction voltage temperature dependence.

The peak detector conducts on the negative RF peaks, generating a dc voltage proportional to the RF power level. This detected dc signal is fed to the input of the loop amplifier, which drives the modulator, which adjusts the RF level to provide the desired output power. This feedback loop is the doubler ALC loop (not the same as the UHF output section ALC loop).

Doubler ALC Loop

The integator has selectable time constants for changing the ALC loop response. If AM or amplitude sweep is selected, the loop bandwidth is 100 kHz. For continuous wave (CW) operation, the ALC loop can be narrowed to reduce noise components. This also improves the third-order intermodulation distortion products because the loop has less bandwidth to respond to an external signal applied to the output.

There are three other modes of operation in the doubler ALC loop. The first is amplitude sweep. Under normal ALC loop operation the vernier's range is from +5 to +16 dBm. In the case of amplitude sweep, the vernier is extended down to a minimum of −15 dBm. This is achieved by the processor's sending digital data to the vernier DAC. The result is that the vernier is swept in a linear or log mode to yield an accurate amplitude sweep over a 20-dB range for a given frequency setting. This function is useful for compression tests on amplifiers and for detector linearity checks.

The next mode of operation is the ALC off mode. Under this condition the ALC loop is opened by a pair of FET switches. One of these FET switches, attached to the output of the ALC loop amplifier, is opened. The second FET switch, which is closed, is connected to the output of the vernier DAC. This allows the vernier DAC to drive the modulator voltage control line directly and set the modulator to a desired attenuation level. This provides the best third-order intermodulation distortion products since the detector can no longer respond to an external signal that falls within the ALC loop bandwidth. These intermodulation products are improved to the level of the nonlinearities found in the power amplifier.

Pulse Operation

The next mode of operation is pulse modulation. Pulse mode in the doubled band also operates with the ALC circuitry turned off. The pulsed RF signal is generated in the UHF output section rather than in the doubled band to provide a much better on/off ratio. The doubler is set to a fixed RF level in the ALC off mode to give the desired output power. As the UHF RF signal level drops, the doubler circuit conversion loss increases drastically since the diodes no longer conduct, thereby improving the on/off ratio by 40 dB. This yields a doubler band on/off pulse specification of 80 dB.

Attenuator Considerations

The HP 8642A and HP 8242B use different types of RF output attenuators. The HP 8642A uses two step attenuators in series, which provide 0 to 145 dB of attenuation in 5-dB steps. One attenuator has up to 85 dB of attenuation and the other has up to 60 dB of attenuation. The reverse power protection circuit is a part of the 60-dB attenuator. Both attenuators use thick-film resistor network attenuator sections on ceramic substrates with TO-5 style miniature relays to switch the various sections in or out. The substrates are mounted inside individual metal housings.

Separation of the attenuators into two separate housings aids in maintaining input-to-output isolation when large amounts of attenuation are desired. For example, when 135 dB of attenuation is desired, stray leakage from attenuator input to output must be lower than 153 dB to maintain an attenuation error of less than 1 dB. Even though the HP 8642A/B has digitally stored corrections for attenuator accuracy, the amount of leakage must be low for the attenuator to be correctable within the vernier constraints of the output section. The low leakage is also required to meet instrument RF leakage specifications.

The HP 8642B also uses two attenuators. However, since the frequency range is higher (2115 MHz), two microwave stripline style attenuators are used to maintain better impedance characteristics, more accurate attenuation, and lower insertion loss. These two attenuators provide 0 to 145 dB in 5-dB steps. One attenuator has up to 70 dB of attenuation and the other has up to 75 dB of attenuation. Both use thin-film resistor networks as attenuator sections and have solenoid-actuated stripline switches to switch the various sections in or out. As in the HP 8642A, the two separate attenuators aid in maintaining isolation. This is even more difficult in the HP 8642B because of the higher frequency range. The reverse power protection circuit in the HP 8642B is on a separate board in another housing.

As mentioned before, the HP 8642A/B has digitally stored correction for attenuator accuracy. There are correction data points approximately every 60 MHz for every 5-dB step in attenuation. This totals about 600 correction points for an HP 8642A and 1140 correction points for an HP 8642B. This sizable amount of data is generated at a level accuracy test station where it is stored in the HP 8642A/B memory. The HP 8642A/B interpolates correction values between frequency data points to get the best level accuracy. At the same level accuracy test station, each HP 8642A/B is verified for level accuracy by measuring levels midway between correction frequencies. This method is sensitive to any leakage problems that might otherwise not be detected by simply checking at the correction frequencies.

Reverse Power Protection

The function of the reverse power protection circuit is to prevent damage to the attenuator and output amplifier caused by the application of excessive RF power to the RF output connector. The circuit detects the signal level at the RF output connector and opens a relay in the signal path when a reverse power situation occurs. During the time required for the relay to respond (approximately 50 μs), a diode limiter circuit prevents more than 1 watt from reaching the attenuator or power amplifier. The design goals for the reverse power protector included, in addition to the protection function, low loss and low VSWR.

To accomplish the design objectives to a frequency of 2100 MHz, a special reed relay was developed. In this relay, the reed capsule forms the center conductor and dielectric of a coaxial transmission line. The outer conductor is formed by a rolled brass shield and a conductive coating on the capsule itself. The relay is soldered into a microstrip circuit, which also contains a limiter and a dc blocking capacitor. The limiter consists of a pair of pin diodes and two Zener diodes which set the limiting level. Limiting begins when the RF level reaches 10 volts peak. A detector senses the level at the limiter and signals the relay to open when the RF level reaches approximately 7 volts peak.

The reverse power protection circuit typically has insertion loss less than 1 dB and VSWR less than 1.25 to 2100 MHz. The maximum power capability is 50 watts in an HP 8642A and 25 watts in an HP 8642B.

Acknowledgments

We would like to thank Art Upham for his tireless leadership and long hours as the HP 8642A/B program manager. Also, we would like to thank Dick Waite, Eric Pirttima, and Alden Forbes of our microcircuit development area and the people of the HP Microwave Technology Division for their assistance in developing HP 8642A/B microcircuits and SAW devices. In addition, we wish to thank our printed circuit designers, assembly and test engineers, and Don Borowski and Tom Yeager for their assistance in development of the output sections. A very special thanks goes to Eric Anderson of our product assurance area for his tireless assistance in rigorous environmental testing of the HP 8642A/B during its development.

Signal Generator Frequency Synthesizer Design

by Thomas R. Faulkner, Earl C. Herleikson, Ronald J. Mayer, Brian M. Miller, and Mark A. Niemann

THE FREQUENCY SYNTHESIZER of the HP 8642A/B Signal Generator is designed to minimize the phase noise, spurious response, and switching speed of the instrument, while optimizing its angle modulation capabilities. This design challenge was met by dividing the frequency synthesis process into component phase-locked loops, which were then individually optimized for their specific function.

The six component phase-locked loops are the time base, the FM loop, the SAWR (surface-acoustic-wave-resonator[1]) loop, the reference loop, the IF loop, and the sum loop. Fig. 1, a general block diagram of the frequency synthesizer, shows the loops' interrelationships.

The time base produces the 10-MHz time base output, a 500-kHz reference for the FM and IF loops, and a 45-MHz reference for the counter, SAWR loop, and the heterodyne reference loop of the output section (see article, page 18). It uses its internal 45-MHz reference oscillator, or it will automatically lock to an externally supplied 1-MHz, 2-MHz, 5-MHz, or 10-MHz reference source.

The FM loop is a 135-MHz reference that provides low-distortion, high-accuracy angle modulation.

The SAWR loop provides the reference loop with three spectrally pure UHF reference frequencies. Using these three references, the reference loop translates the FM loop's angle modulation into six UHF frequencies.

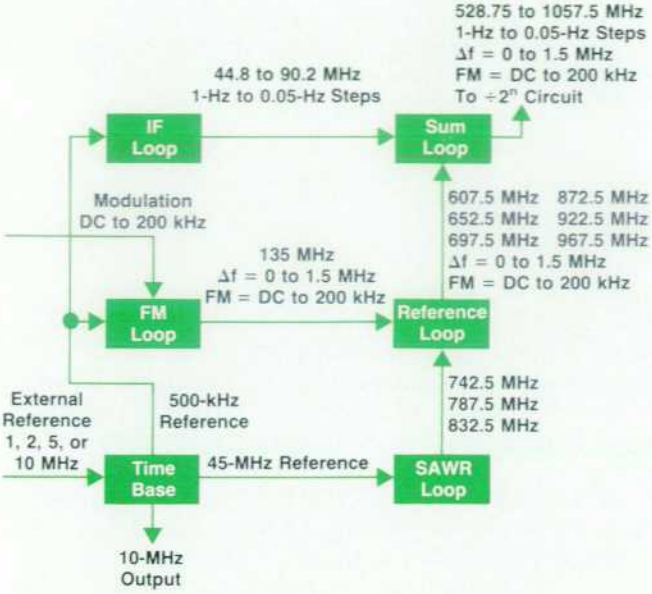


Fig. 1. *Six phase-locked loops make up the frequency synthesizer section of the HP 8642A/B Signal Generator.*

The IF loop is a fractional-N synthesizer that produces a spectrally pure VHF reference from 44.8 to 90.2 MHz in steps as small as 0.05 Hz.*

Using the IF reference frequencies, the sum loop translates the six reference loop frequencies to produce the fundamental octave of the instrument. Thus the sum loop output has the full angle modulation capability of the FM loop, the frequency resolution of the IF loop, and nonharmonically related spurious levels of less than −100 dBc for carrier offsets greater than 10 kHz maintained by all loops.

Loop Structures

The time base (Fig. 2) and SAWR (Fig. 3) loops are sampling phase-locked loops. They use sampling phase detectors to multiply the reference frequency up to the loop's output frequency. The output of a sampling phase detector is a voltage proportional to the phase difference of the sampled output frequency and the reference frequency. The detector's output is integrated, then used to control the relative phase of the loop's voltage-controlled crystal oscillator (VCXO), producing a phase-locked output.

The FM (Fig. 4) and IF (Fig. 5) loops are divider phase-locked loops. They use digital frequency dividers to divide the voltage-controlled oscillator's (VCO's) output frequency down to the reference frequency, which is fed into the digital phase/frequency detector. The detector's output is integrated and sent to the VCO's control voltage input. If the reference and divided VCO signals are at different frequencies, a dc offset voltage will be produced that forces the integrator to move the VCO toward the reference frequency. Once the reference and divided VCO signals have reached the same frequency, the detector's output is proportional to the phase difference of the two signals and forces the loop output to be phase-locked to the reference. The IF reference loop has the additional design constraint of a 0.05-Hz frequency resolution, which was met by using a fractional-N phase-locked loop.

The fractional-N technique allows the use of effective noninteger divide numbers. It involves switching between two integer divide numbers with varying duty cycles. Several additions are made to a conventional phase-locked loop to make it a fractional-N loop.

When the divide number is not an integer, the divider output does not equal the reference frequency. This causes an increasing phase offset, which sends more current into the loop integrator. This is compensated for by adjusting the amount of phase correction current. The output of the integrator is shown in Fig. 6. The phase detector causes a ramp up in voltage. The phase correction current causes a ramp down. The phase correction is adjusted to make these two ramps equal in length.

The phase difference between the two phase detector inputs is accumulated digitally in the fractional-N IC and applied to the phase correction current sources. This phase correction is limited to 360° by practical limitations of the phase detector hardware. When one complete cycle of extra phase is accumulated, the fractional-N IC instructs the divider to "swallow" one pulse of the VCO output. This gives the signal applied to the phase detector an average fre-

*The normal resolution of the IF loop is 1 Hz in the undoubled band and 0.5 Hz in the doubled band (above 1057.5 MHz in the HP 8642B). A special function provides resolutions of 0.1 Hz and 0.05 Hz, respectively.

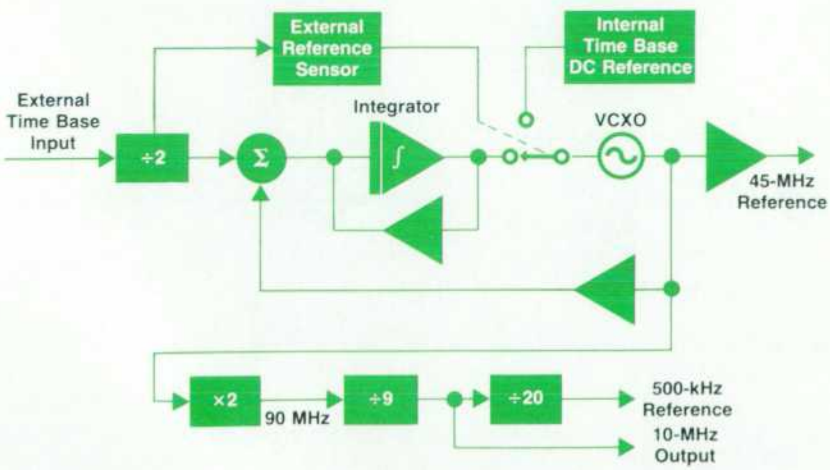


Fig. 2. *Time base loop block diagram.*

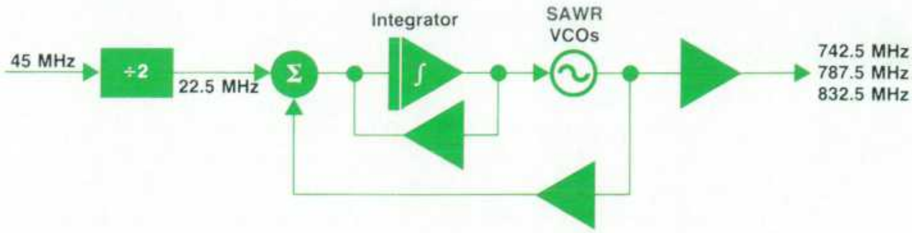


Fig. 3. *SAWR (surface-acoustic-wave-resonator) loop block diagram.*

quency of 100 kHz.

The accuracy with which the up and down ramps can be equalized determines the level of sidebands on the loop output. If these ramps are different the output appears to jump between two frequencies. The HP 8642A/B hardware is capable of correction that results in spurious levels of −60 to −65 dBc. This is further reduced by loop filtering, as explained later.

The sum (Fig. 7) and reference (Fig. 8) loops are summing phase-locked loops. They produce the sum or difference of two reference frequencies with minimal spurious signals by mixing the loop's UHF output with a UHF reference to produce an intermediate frequency signal. This signal is then filtered and amplified and sent to a phase detector. The phase detector's output is a voltage proportional to the phase difference of the detector's VHF reference and the intermediate frequency signal. The detector's output is then integrated and used to control the loop's VCO. To ensure that the loop locks to the correct mixer sideband, the VCO is pretuned to within 7.5 MHz of the loop's output frequency. The trade-off between phase noise and spurious outputs is optimized by adjusting the VCO's tuning sensitivity to produce a constant loop bandwidth of 1.8 MHz.

Minimizing Phase Noise

Within its bandwidth, a phase-locked loop will track the effective noise of its reference signals. This effect can make a low-noise voltage-controlled oscillator more noisy, or a noisy VCO more quiet, depending on the loop bandwidth, the open-loop VCO noise performance, and the effective noise of the reference signal. The effective reference noise for a frequency-multiplying loop is the reference noise increased by the multiplication factor. The effective reference noise of a summing loop is the sum of the references' noise. Outside of its bandwidth, the noise of a phase-locked loop is the sum of the open-loop VCO noise, the buffer amplifier noise floor, and the effective reference noise lowered by −20 log (carrier offset frequency ÷ loop bandwidth) dB.

The time base and the FM, SAWR, and IF loops are all multiplier-type loops, and have in common narrow loop bandwidths and VCOs with narrow tuning ranges and low phase noise. Narrow loop bandwidths prevent multiplied reference noise from degrading the VCO noise. The sum and reference loops are summing-type loops and have in common wide loop bandwidths and moderate-noise, wide-tuning-range VCOs.

All the oscillators in the instrument are designed for low noise.[2] For its particular application, each oscillator is optimized with the lowest practical white noise floor and with a resonator of the highest practical Q and lowest practical 1/f noise corner. Degradation of resonator Q from resonator switching circuitry has been eliminated by switching entire oscillators instead of individual resonators.

The SAWR loop employs three surface-acoustic-wave-resonator (SAWR) oscillators. The SAW resonators were specially developed by HP Laboratories to meet the low

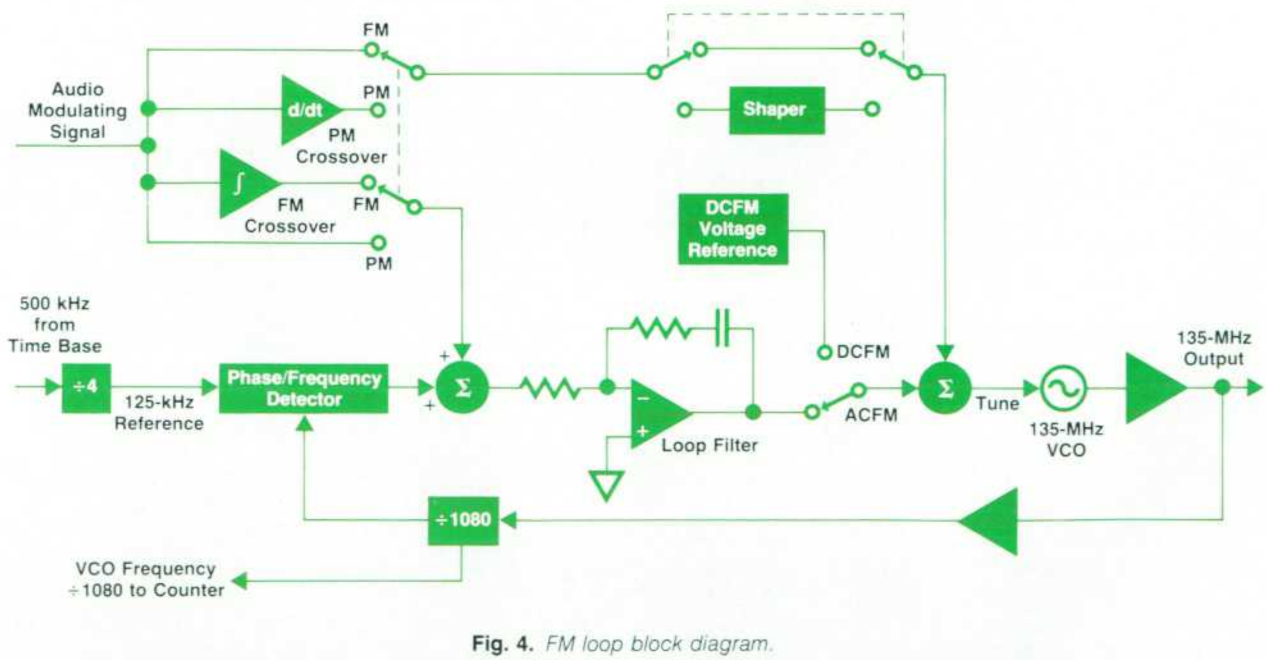


Fig. 4. *FM loop block diagram.*

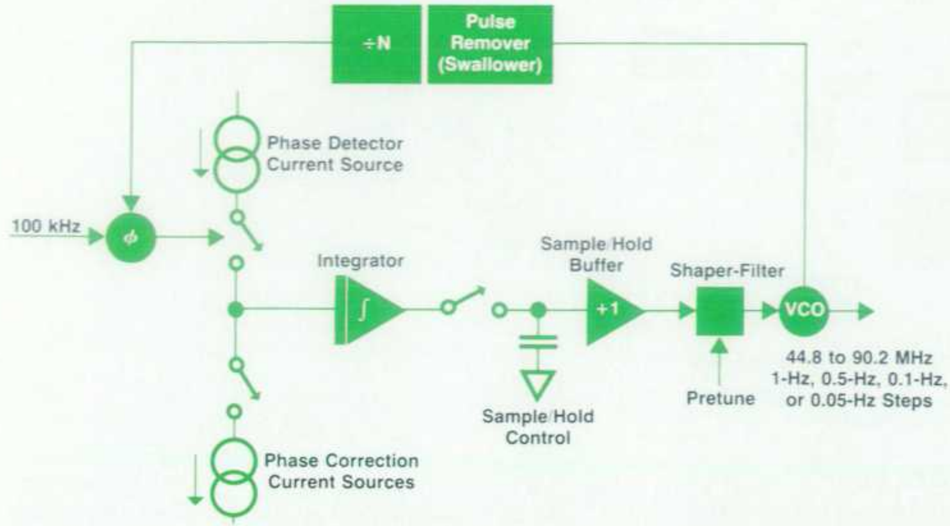


Fig. 5. *IF loop block diagram. This loop is a fractional-N loop.*

phase noise and frequency pull requirements of the HP 8642A/B at UHF frequencies. The SAW resonators are multiple-cavity resonators and provide a low source resistance (R_s) with transverse modes far from the center frequency. The low R_s provides a wide frequency pulling range (>300 ppm) with inexpensive varactors. Low R_s also minimizes loop-gain loss without the need for matching transformers, thus reducing frequency drift caused by external component tolerances.

The FM, IF, sum, and reference loops all use varactors especially selected for high Q and low 1/f noise corner. A well-filtered 50V power supply operates the varactors in the upper two thirds of their voltage range to maximize their Q. VCO sensitivity to control-line noise is minimized by limiting VCO tuning sensitivity.

To meet the instrument noise performance goals, six VCOs are used in the IF loop, two in the reference loop, and four in the sum loop. The IF and FM loop VCOs use inductor/varactor resonators, with inductor geometry optimized for maximum Q in the space available. The varactors are preselected for low noise by testing them in a VCO inside a phase-locked loop. The gain stages for these oscillators consist of a source-follower and a common-gate amplifier. The common-gate stage provides the necessary gain to support oscillation. The source-follower provides an impedance buffer to reduce loading of the resonant circuit by the common-gate stage. This increases the loaded Q of the resonator, which improves the phase noise performance. The feedback is obtained with capacitors used as impedance transformers. This minimizes loading, sets the proper loop gain, and provides the necessary phase shift for oscillation.

The sum and reference loop VCOs use transmission-line/varactor resonators, built on Teflon™/glass printed circuit boards. Their circuit configuration is that of a Hartley oscillator modified to operate with high Q at high frequencies (Fig. 9). At frequencies above f_{hfe} (3-dB corner of h_{fe}), a transistor's β (h_{fe} in the common-emitter configuration) has an additional 90° of phase lag because of base diffusion capacitance. This phase lag of the transistor at high frequencies is compensated by the phase lead of the series capacitance of the base and collector. The amplifier circuit now has the necessary 180° phase shift which, when added to the 180° phase shift of the resonant circuit, produces the 0° phase shift necessary for oscillation.

High Q is achieved by tapping down on the transmission line inductors with both the base and collector, which have approximately 15Ω and 50Ω load and source impedances, respectively. This leaves the Q to be set primarily by the tunable element of the tank circuit, the varactor. The unloaded Q is greater than 100, and the loaded Q is greater than 60.

Minimizing Spurious Responses

Several design procedures ensure that the HP 8642A/B meets its design goal that all nonharmonically related spurious outputs be less than −100 dBc at offsets greater than 10 kHz from the carrier. To prevent spurious leakage and electromagnetic interference (EMI), beryllium-copper spiroshield gaskets and conductive elastomer are used in the die-cast aluminum housings. Noncritical cables are triple-shielded coax, critical RF cables are semirigid coax, and all power supply and digital control lines through module walls are bypassed with feedthrough filters.

Steel support frames and MuMetal™ in critical areas prevent modulation of sensitive narrow-bandwidth phase-locked loops via magnetic coupling from the power transformer. The time base, FM, IF, and SAWR loops, and the high-stability 10-MHz reference (Option 001) are shock-

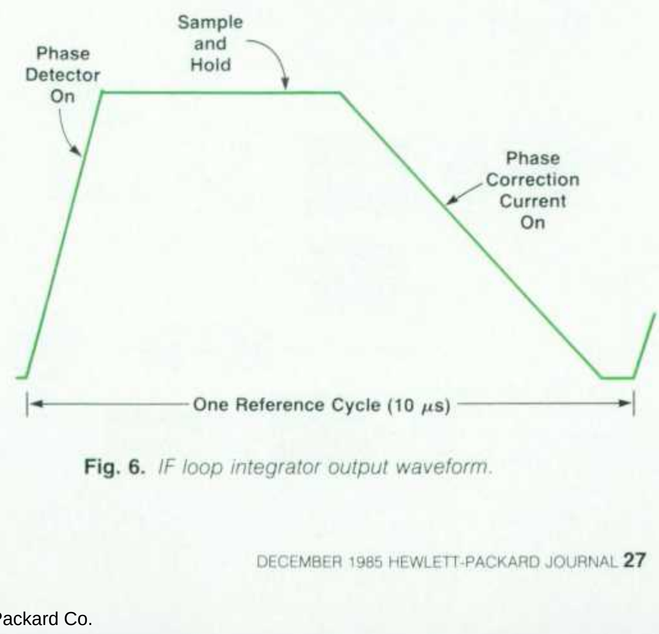


Fig. 6. *IF loop integrator output waveform.*

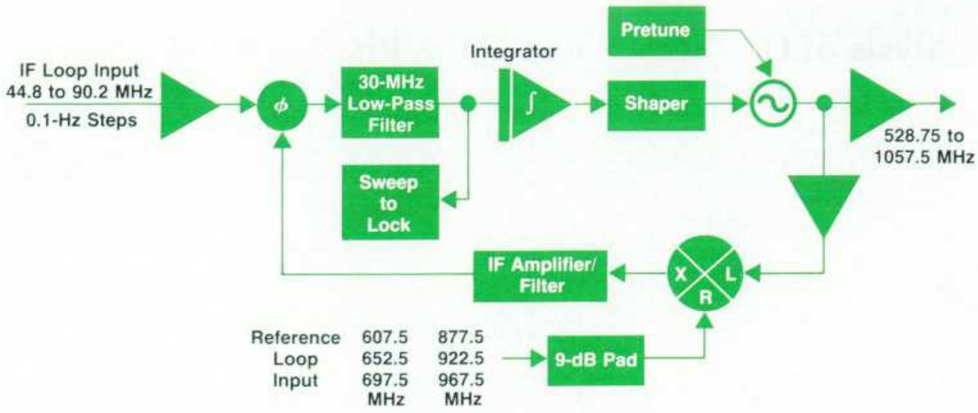


Fig. 7. *Sum loop block diagram.*

mounted in the instrument to prevent mechanical vibration from modulating sensitive VCOs. The IF and FM oscillator inductors are dampened with vibration-absorbing foam to reduce microphonically induced FM.

Amplifiers in the feedback path of each loop are used to prevent spurious signals from appearing on the loop outputs. Sampling spurious from the phase detectors of the time base and SAWR loops, divider spurious from the FM and IF loops, and UHF reference and phase detector spurious in the sum and reference loops are thus eliminated. Output path buffer amplifiers are used to prevent signals from moving backwards through the synthesizer and producing spurious signals in otherwise spectrally pure references. The buffer/limiters used for spurious isolation are designed to prevent baseband noise from upconverting around the carrier. This is accomplished by diplexing each amplifier stage output such that low-frequency noise is terminated in a 50Ω load and the desired signal is passed on to the next stage. VCO spurious resulting from phase detector feedthrough and harmonics is attenuated by loop filters and integrators. Phase-locked loops also act as low-pass filters. Spurious signals generated inside the loop bandwidth remain constant, while those generated outside the bandwidth are attenuated by -20 log (spurious offset frequency ÷ loop bandwidth) dB. In the IF loop, the fractional-N divider produces spurious of -60 to -65 dBc. A 200-Hz loop bandwidth and a one-pole low-pass filter at 1 kHz provide an additional 54 dB of spurious attenuation at 10 kHz, producing a total spurious performance of less than -110 dBc at offsets greater than 10 kHz.

The sum and reference loops' mixer spurious outputs are unfilterable within the loops' 1.8-MHz bandwidths. The mixers were especially built and selected for low spurious. Impedance matches at all ports, power levels at the LO and RF ports, and minimal harmonics at the RF port are all carefully maintained to avoid degrading mixer spurious performance. Mixer output power is optimized to provide minimum spurious with minimal phase noise degradation.

Minimizing Frequency Switching Time and Phase Acquisition Time

The instrument's frequency switching time is set by the IF loop to typically 70 ms, during which time the SAWR, reference, and sum loops are also switched. The FM and time base loops do not change frequency during standard instrument operation. Switching and acquisition times are inversely proportional to the loop's bandwidth. This limitation is overcome in the IF and SAWR loops by widening the loop bandwidths during phase acquisition. The IF loop increases switching speed by pretuning the VCOs, and widens loop bandwidth using a speedup circuit that reduces the attenuation in the loop's lead/lag filter whenever there is a rapid change in the integrator output voltage. The SAWR loop senses an out-of-lock condition and increases

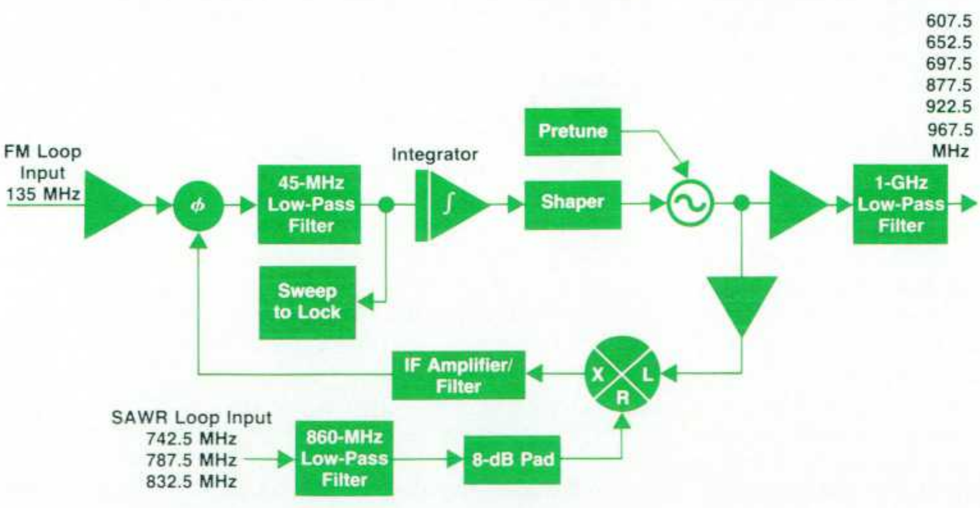


Fig. 8. *Reference loop block diagram.*

Computer Analysis of Oscillator Loop Gain, Phase, and Q

One of the reasons that high-frequency oscillator design is considered a black art is that the open-loop gain and phase have been very difficult to measure. The main reason for this difficulty is that the gain stage (transistor) has input and output impedances that depend on the source and load impedances. The source and load impedances are a function of the feedback network (resonator) which changes radically through the region of resonance.

For a feedback oscillator design, the following method allows one to characterize oscillator performance by the direct measurement of the s-parameters of the open-loop oscillator. To calculate open-loop gain, first rewrite the circuit of Fig. 9c, page 30 as an ideal amplifier with a feedback network. This can be done by the following three steps (see Fig. 1):

1. Break the loop and measure the s-parameters (Fig. 1a).
2. Convert the s-parameters to y-parameters to yield ideal amplifiers (Fig. 1b).
3. Close the loop and redraw it as an ideal amplifier with feedback (Fig. 1c).
4. Open loop gain $= \dfrac{y_{12}+y_{21}}{y_{11}+y_{22}}$

$$Q = (f_o/2)(d\phi/df)$$

where f_o = carrier frequency and $d\phi/df$ = rate of change of the open-loop phase (radians) with frequency.

The key to the success of this method is that all of the feedback paths in the oscillator must be broken. Otherwise, the voltage dependent current sources (y_{12} and y_{21}) will not be completely isolated from the load (y_{11} and y_{22}). The extreme case of this would be to break the loop between a negative-resistance device and its load. In this case, $y_{12}+y_{21}=0$ and $y_{11}+y_{22}<0$.

A linear frequency-domain circuit analysis program was used extensively to predict oscillator noise performance of the HP 8642A/B. This program models an oscillator as a feedback control system with a complex pole pair on the $j\omega$ axis. All of the components' noise models are used to model the oscillator. Then, to model oscillation, the gain around the loop is adjusted to 1 where the phase shift is zero degrees. Output phase noise spectral density is the ratio of the oscillator output power (measured experimentally or predicted with another program) to the peaked noise floor predicted by this method.

These computer analysis techniques were used in the design of all the oscillators to optimize and ensure the instrument's performance.

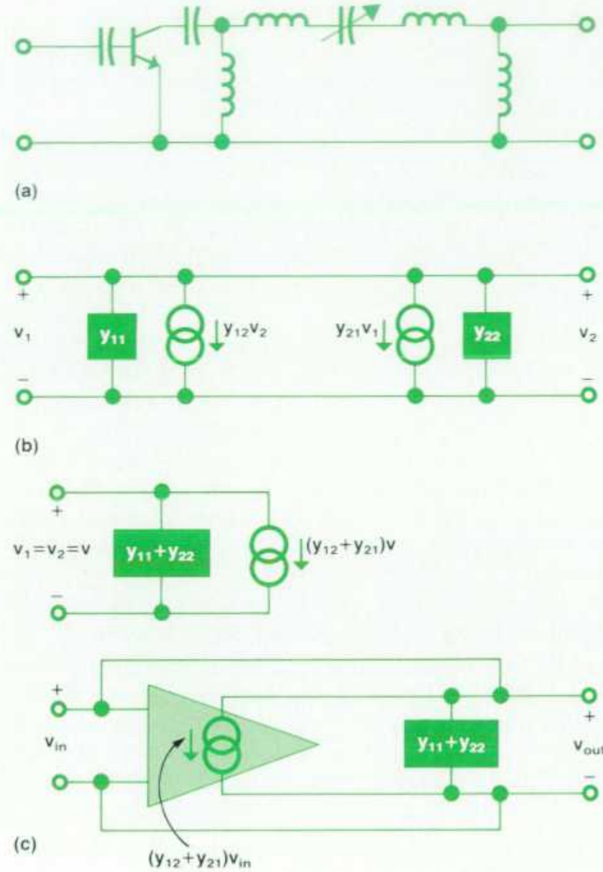


Fig. 1. *(a) Oscillator circuit drawn as ideal amplifier with feedback loop opened. (b) S-parameters converted to y-parameters. (c) Loop closed and circuit redrawn as an ideal amplifier with feedback.*

the integrator gain, which increases loop bandwidth.

The phase detectors of the time base, SAWR, sum, and reference loops achieve phase lock by sweeping the VCO through the desired output frequency by integrating an offset current at the integrator input. In the time base and SAWR loops, the offset is generated by a positive feedback amplifier, which becomes astable without the negative feedback generated by phase locking. The sum and reference loop out-of-lock circuitry triggers a pair of nonretriggerable one-shot multivibrators to control the injection of their offset currents. This forces the integrator output to ramp positive, then negative. The amplitude of the offset currents is one third of the available current out of the phase detector. Thus, when the loop sweeps through the desired output frequency it becomes locked, and the offset currents are overridden until they are shut off.

Angle Modulation

The instrument's angle modulation capability is generated in the FM loop, and must pass through the reference and sum loops without being degraded. Distortion in the sum and reference loops is minimized by wide loop bandwidths and by optimizing the frequency of the loop integrator's zero to approximately 8 kHz. The loop phase detectors are run at very high levels, producing a linear phase slope to minimize modulation distortion.

The FM loop operates at a single frequency of 135 MHz to optimize high-accuracy, low-distortion angle modulation and phase noise performance. The FM loop's VCO optimizes the trade-off between high tuning sensitivity for low-distortion FM and low sensitivity to prevent modulation by audio-path noise. The FM loop VCO typically produces less than −55 dB (0.18%) distortion for 100-kHz deviation. Switching into low-distortion mode further reduces FM distortion. This mode employs a shaper using a JFET in its saturated, constant-resistance region to predistort the modulating signal, cancelling the distortion generated in the VCO. At a small cost to the FM loop's noise performance, switching into low-distortion mode improves FM distortion to typically better than −80 dB (0.01%) at a 1-kHz rate and 100-kHz deviation. Performance degrades slightly with increased modulation frequency, primarily because of limitations in the audio path.

FM distortion from nonlinear operation of the loop's phase/frequency detector at low-rate, large-deviation FM is reduced by limiting the phase detector's deviation to ±1 radian. Because the phase detector operates at 1/1080 of the VCO frequency, the multiplying phase-locked loop produces a corresponding ±1080-radian deviation at the loop's output.

Modulation is applied at two points in the loop. These are the phase detector output and the VCO input (see Fig. 4). Signals summed with the phase detector output cause phase modulation at the loop output. However, there is a low-pass characteristic between the voltage applied and the phase modulation obtained. The 3-dB point of the low-pass response is the 3-dB loop bandwidth, approximately 100 Hz. Consequently, without a crossover network, phase modulation is possible only from dc to 100 Hz.

Frequency modulation is obtained by summing a signal with the loop filter output and applying it to the VCO input. The frequency modulation obtained is rolled off by the phase-locked loop inside the loop bandwidth. Since the FM loop bandwidth is approximately 100 Hz, without a crossover network, frequency modulation would be possible only for modulation rates greater than 100 Hz.

The FM and PM crossover networks rely on the derivative relationship between instantaneous frequency and phase:

$$f(t) = d\phi(t)/dt$$
$$\phi(t) = \int f(t)dt.$$

The phase modulation crossover network is a differentiator whose output,

$$V_{PMX}(t) = dV_{in}(t)/dt,$$

is applied to the VCO input. V_{PMX} is the phase modulation crossover output voltage. The resulting FM occurs outside the loop bandwidth and is proportional to $V_{PMX}(t)$, that is,

$$f(t) = C_1V_{PMX}(t)$$

where C_1 is a constant. This is equivalent to phase modulation of

$$\begin{aligned}\phi(t) &= \int C_1V_{PMX}(t)dt\\ &= \int C_1[dV_{in}(t)/dt]dt\\ &= C_1V_{in}(t).\end{aligned}$$

The phase modulation crossover network allows 100 radians of phase deviation from dc to 15 kHz (3-dB bandwidth).

The FM crossover network is an integrator. The FM crossover output voltage is

$$V_{FMX}(t) = \int V_{in}(t)dt.$$

This signal is summed with the phase detector output and causes phase modulation proportional to $V_{FMX}(t)$, i.e.,

$$\phi(t) = C_2V_{FMX}(t)$$

where C_2 is a constant. This phase modulation occurs inside the loop bandwidth and is equivalent to frequency modulation of

$$\begin{aligned}\Delta f(t) &= d[C_2V_{FMX}(t)]/dt\\ &= d[C_2\int V_{in}(t)dt]/dt\\ &= C_2V_{in}(t).\end{aligned}$$

The FM crossover circuit has two modes of operation. In normal operation the crossover network approximates an ideal integrator down to 3 Hz and provides better than 5% flatness from 20 Hz to 100 kHz. The crossover feedback is altered in low-rate-FM mode and the integrator approximation is extended to 0.3 Hz. The low-rate-FM mode allows phase-locked FM with a 3-dB bandwidth of 0.4 Hz to 200 kHz, at the expense of increased settling time in response to changes in the modulating signal.

For extremely low-rate FM or for direct, external frequency control of the HP 8642A/B, dcFM mode is available. In dcFM mode, the FM VCO is not phase-locked. The FM

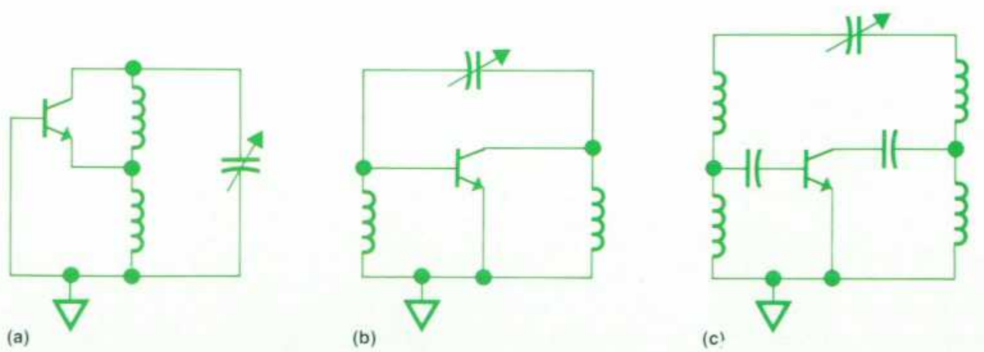


Fig. 9. *(a) Hartley oscillator. (b) Hartley oscillator redrawn. (c) Modified Hartley oscillator.*

phase-locked loop is broken at the loop filter output and the VCO tuning voltage is obtained from a low-noise, high-stability dc reference instead of the loop filter output (Fig. 4). The dc reference provides a very stable voltage to minimize unlocked oscillator drift. The VCO is temperature compensated and the unlocked drift rate is less than 4 kHz/hr after warmup.

Unfortunately, the dc reference cannot provide a voltage with sufficient accuracy to set the VCO at exactly 135 MHz in dcFM operation. The VCO frequency can be in error by as much as 200 kHz in dcFM mode. Because this frequency offset is undesirable, the HP 8642A/B's internal counter is used to restore the instrument's output frequency. Upon entering dcFM mode, the microprocessor directs the counter to count the output frequency of the unlocked FM loop VCO. The microprocessor calculates the frequency error in the unlocked FM loop and then adjusts the frequency of the fractional-N loop to compensate for the FM loop error at the instrument's output. After compensation, the frequency offset error at the instrument's output is typically less than 50 Hz when dcFM is selected.

A special function is provided to initiate frequency compensation of the unlocked FM oscillator at any time, to correct for oscillator drift.

Acknowledgments

The authors wish to thank the essential Art Upham for his program management and long hours, Skip Crilly, Eric Anderson, Jeanette Bachman, Morris Chase, Jerry Hayes, and the Santa Rosa Technology Center for their support, ideas, and assistance, and Fred Ives, Tim Carey, Greg Taylor, Roger Muat, and Bob Burns, the original HP 8642A/B design team.

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Audio Modulation Section for an RF Signal Generator

by Gary L. Tong

THE HP 8642A/B Signal Generator can produce AM, FM, PM, and pulse modulation. Its modulation capabilities are intended to satisfy as many standard applications as possible, but their performance and versatility allow the user to generate a wide variety of signals to satisfy nonstandard and laboratory needs.

HP 8642A/B modulation capabilities include an internal, low-distortion, variable-modulation oscillator that covers 10 Hz to 100 kHz. The signal from this oscillator can be used either internally for AM or FM (may be simultaneous, if desired) or externally as a low-frequency source. It can also be used internally and externally simultaneously. Having an internal modulation source eliminates the need for an additional modulation source for many applications, thus saving space and money. As an external source, the modulation oscillator offers adjustable frequency and amplitude, providing the user with a flexible low-frequency source for a wide range of applications.

The HP 8642A/B can also generate multimode modulation such as simultaneous AM and FM, internal FM and external AM or pulse, and many other combinations of AM, FM, PM, and pulse with internal and external sources. These combinations can be very useful for customers doing tests on equipment such as receivers, or doing tests to determine cross sensitivities to modulation formats.

The HP 8642A/B's AM and pulse modulators are described in detail in the article on the output section, page 18, and the FM modulator is described in the article on page 24.

Audio Modulation Section

The purpose of the modulation section is to amplify or attenuate audio signals accurately while contributing as little noise, distortion, and dc offset to those signals as possible. The sources of these audio signals include externally applied inputs and the internal low-distortion audio oscillator. The outputs of the modulation section amplifiers are routed to other sections of the instrument where the actual AM, FM, pulse modulation, and phase modulation of the instrument's RF carrier take place. The modulation section allows both ac and dc coupling of external audio inputs as well as multiple-mode modulation capabilities such as simultaneous internal and external AM and FM with 1-dB modulation bandwidths in excess of 100 kHz. The internal audio oscillator covers the frequency range of 10 Hz to 100 kHz, and has a typical settling time of 10 to 20 cycles when frequency is changed. The oscillator's distortion is better than 0.01% for rates below 15 kHz (0.1% for all rates), and the oscillator's output is also available outside the instrument through the **MOD OUT** port. A block diagram of the modulation section is shown in Fig. 1.

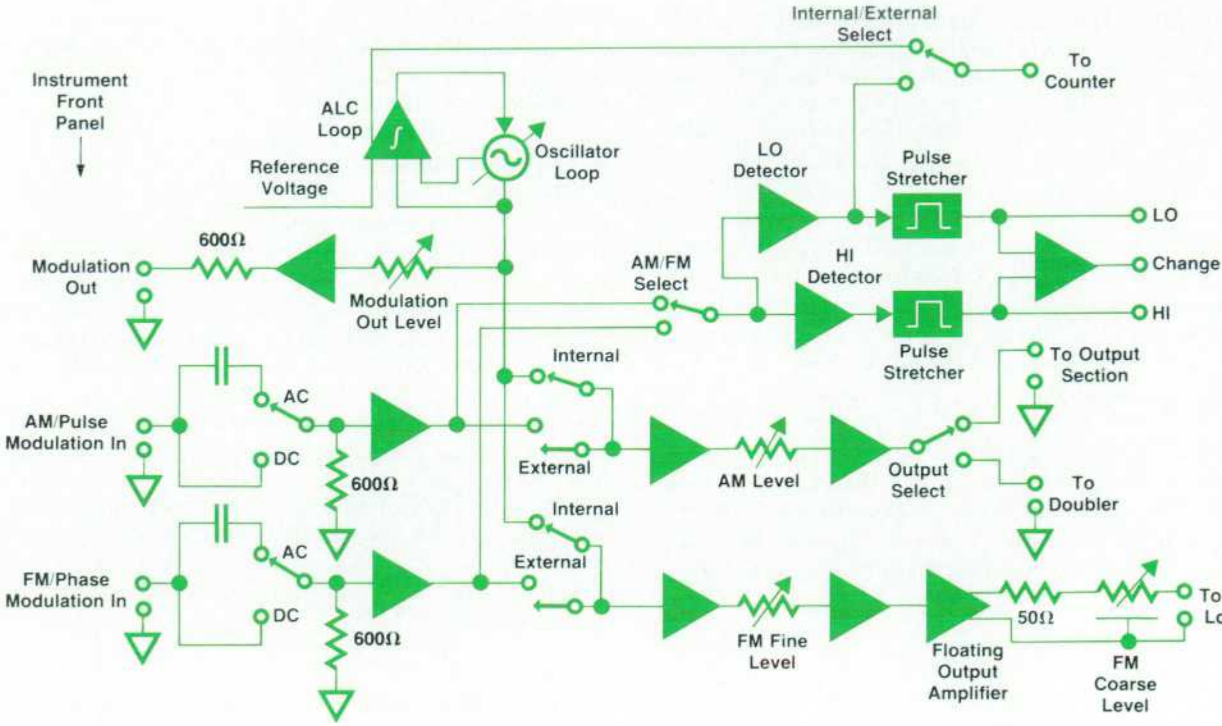


Fig. 1. *HP 8642A/B modulation section block diagram.*

Special Considerations for High-Performance FM

Much attention was paid to providing high-quality, high-deviation, low-distortion FM. For example, the FM section provides low-distortion FM and 50-dB stereo separation for use in FM broadcast and laboratory applications. Very low-rate, phase-locked FM accommodates subaudible frequency-shift keying. The FM oscillator can be unlocked and dc-coupled to accommodate external phase locking.

Because of the large dynamic range of audio signals that must be supplied to the instrument's FM modulator, extra precautions must be taken to minimize the effects of noise and ground loops at the modulation section's FM output. To keep the noise contribution of the modulation section as small as possible when low FM deviations are required, the FM output amplifier is followed by a three-stage attenuator, as shown in Fig. 2.

The gain of this attenuator can be varied from 0 db to −63 dB in 9-dB steps while maintaining a low and fairly constant output resistance of 50Ω to keep resistor noise negligible. The input resistance of this configuration is, of course, not constant as a function of attenuator setting, but this is not necessary since the attenuator is driven directly with an operational amplifier. In fact, the higher the input resistance, the better. High-reliability two-coil latching SPDT electromechanical relays are used in the design to achieve minimum relay power consumption, consistently low contact resistance, and long attenuator lifetime. The low side of the attenuator is connected to the floating ground output of the FM output amplifier to minimize pickup of ground loop signals.

The operation of the modulation section FM output amplifier is also shown in Fig. 2. Given that V_1, V_2, and

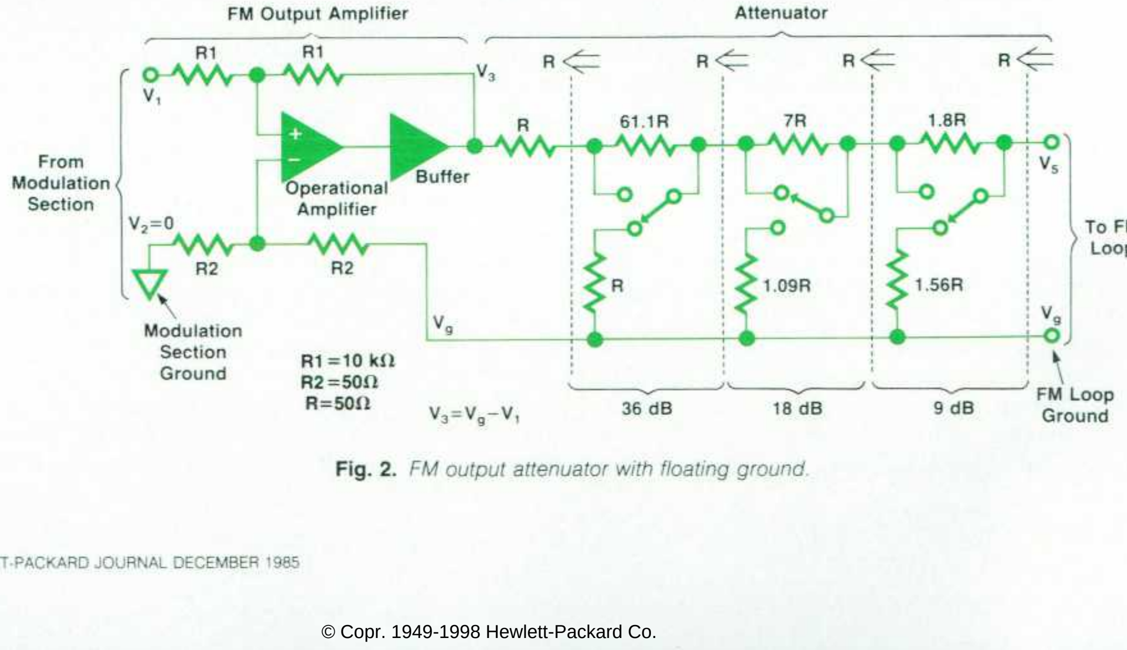


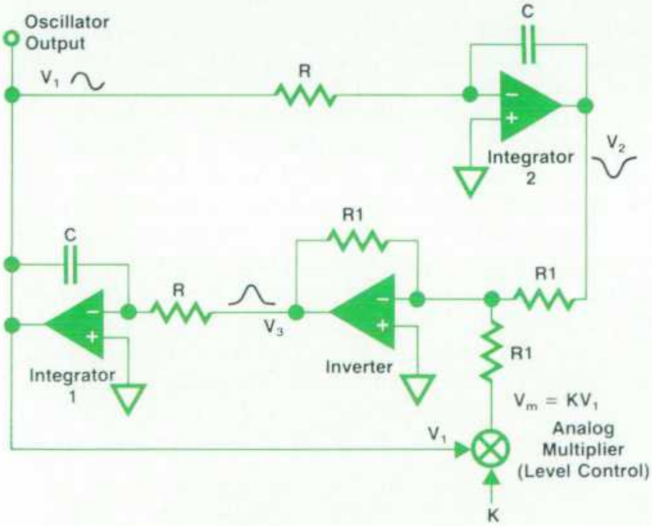
Fig. 2. *FM output attenuator with floating ground.*

V_g are inputs to the operational amplifier and V_3 is the output, it can be shown from Fig. 2 that $V_3 = V_g + V_2 - V_1$. Now, let V_1 and V_2 be the modulation section audio and ground connections to the operational amplifier, respectively, let V_3 be the output to the instrument's FM modulator, and let V_g be the FM modulator's ground. Taking the modulation section's ground as a reference, V_2 becomes zero, V_1 becomes the audio signal, and V_g represents the difference in ground potentials between the FM modulator and the modulation section's ground. From Fig. 2, V_3 now becomes $V_g - V_1$, and the voltage across the FM modulator itself is $V_3 - V_g$, or $-V_1$ with no ground-loop component.

Low-Distortion State Variable Oscillator[1]

The purpose of the modulation section's internal oscillator is to generate low-distortion audio signals with rates from 10 Hz to 100 kHz. These signals can be used by the instrument for internal AM, FM, pulse modulation, or phase modulation of the RF carrier. This audio signal is also available at the instrument's **MOD OUT** jack as a clean 600Ω audio source. The heart of the oscillator is the oscillator loop, which is shown in Fig. 3.

The oscillator loop consists of two inverting integrators and an inverting unity-gain amplifier connected in a loop. An inverting operational amplifier oscillator design was chosen to minimize distortion contributions from nonlinearities in operational amplifier input differential pair stages by keeping all operational amplifier inputs at zero volts. The analog multiplier provides an alternate feedback path in the oscillator loop and is used for level control. With the gain of each integrator equal to $-1/sRC$, the gain of the inverting amplifier equal to -1, and the gain K of



For $K=0$,

Loop Gain $= E(s) = \dfrac{-1}{s^2R^2C^2}$

Closed-Loop Gain $= \dfrac{E(s)}{1-E(s)} = F(s) = \dfrac{-1}{1+s^2R^2C^2}$

Angular Oscillation Frequency $= \omega_o = \dfrac{1}{RC}$

For $K \neq 0$,

Closed-Loop Gain $= F(s) = \dfrac{-1}{s^2R^2C^2 - sKRC + 1}$

Fig. 3. *Oscillator loop with level control.*

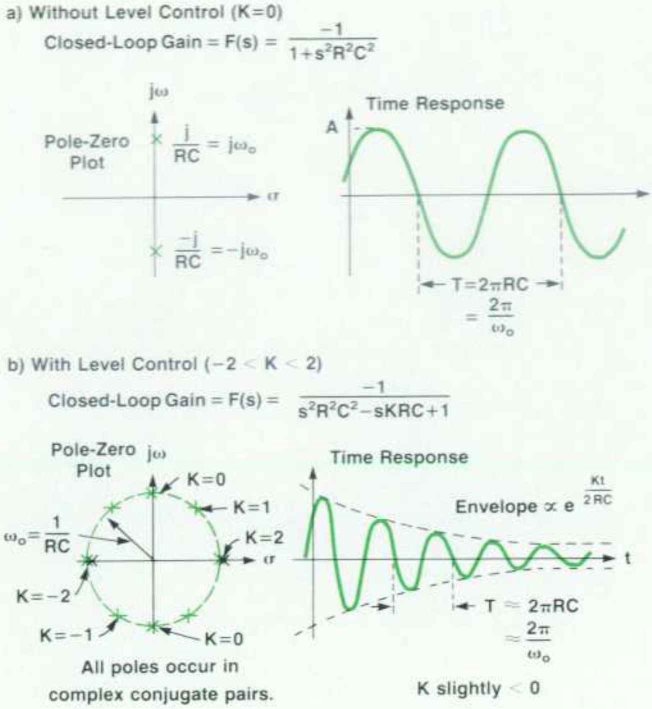


Fig. 4. *Oscillator loop closed-loop response.*

the analog multiplier set to zero, the closed-loop gain F(s) can be shown to be $-1/(s^2R^2C^2+1)$. This response has two poles, located at $s = j/RC$ and $s = -j/RC$. In the time domain, this corresponds to a single sinusoid of angular frequency $\omega_o = 1/RC$ and amplitude A equal to an unknown constant (see Fig. 4a).

The modulation section oscillator's frequency is changed by varying the resistor and capacitor values that determine the gains of the two integrators in the oscillator loop. The frequency range of 10 Hz to 100 kHz is broken into five bands by using FET switches to connect different values of capacitors across the integrators, and CMOS multiplying DACs (digital-to-analog converters) are used as the variable resistors to provide fine frequency resolution within each band.

In reality, the three operational amplifiers in the circuit exhibit noninfinite gain at dc and excessive high-frequency phase shifts. Depending on the oscillator's rate, these nonidealities will produce either a positive or negative feedback effect in the oscillator loop's closed-loop gain, causing the oscillator's output to become an exponentially growing or decaying sinusoid instead of one with a constant amplitude. Some sort of external feedback control is necessary to stabilize the oscillator's output amplitude.

By allowing the analog multiplier gain K to be nonzero in the oscillator loop circuit of Fig. 3, an additional feedback path is provided and the oscillator's output level can be controlled. The closed-loop gain of the circuit, F(s), now becomes $-1/(s^2R^2C^2 - sKRC + 1)$. For $-2 < K < +2$, this new response has two poles, located at

$$s = [K + j(4-K^2)]^{1/2}/2RC$$

and at

$$s = [K - j(4-K^2)]^{1/2}/2RC$$

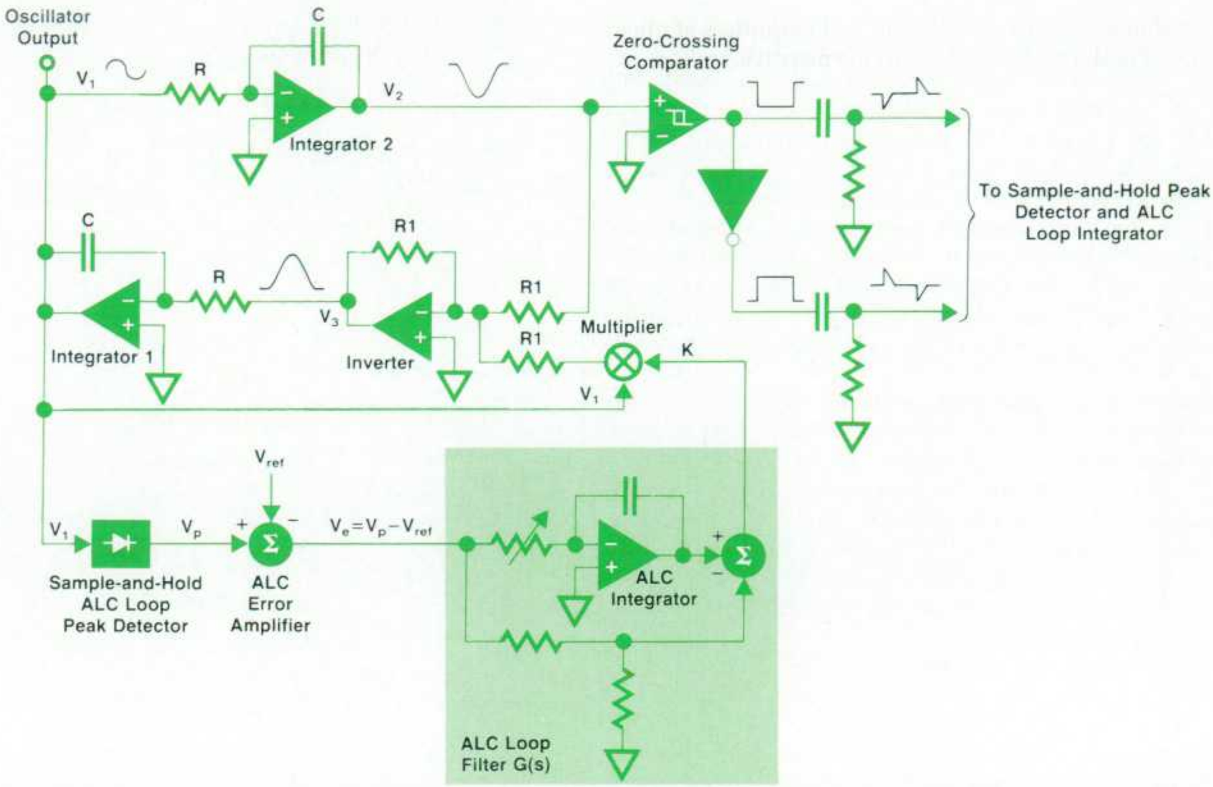


Fig. 5. *Audio oscillator with ALC loop.*

For $|K| << 2$, this corresponds to a time domain response that is a sinusoid of angular frequency $\omega_o = 1/RC$ and an amplitude A proportional to $\exp(Kt/2RC)$, as shown in Fig. 4b. Thus, by varying the parameter K, the output amplitude of the oscillator loop can be made to grow or decay exponentially.

Oscillator ALC Loop

The purpose of the oscillator ALC loop is to measure the level of the oscillator's output, compare this to the desired level to generate an error voltage, and convert this error voltage into a control voltage, K, which sets the gain of the analog multiplier in the oscillator loop feedback path to make the actual oscillator output level equal to the desired level. A block diagram of the oscillator loop along with the ALC loop is shown in Fig. 5.

A sample-and-hold peak detector is used to measure the oscillator's output level. One advantage of this type of detector is a fast response time, which helps to minimize oscillator settling time. Another advantage is the absence of detector output ripple when the oscillator's level has settled, meaning no postdetector filtering is necessary to reduce ALC loop contributions to oscillator loop distortion. The detector circuit is shown in Fig. 6. Diode CR1 and capacitor C_d form the actual peak detector, with operational amplifier U2 buffering the output. U1 is used to remove the forward voltage drop at CR1 by comparing U2's output, fed back through resistor R_f, to the original signal to be detected, which comes from the first integrator of the oscillator loop. When the input signal reaches a positive peak, FET switch S2 is closed momentarily, transferring the detected peak voltage to hold capacitor C_h. CR2 provides a feedback path around U1 when CR1 is back-biased, and C_c is necessary to prevent U1 from oscillating when CR1 is

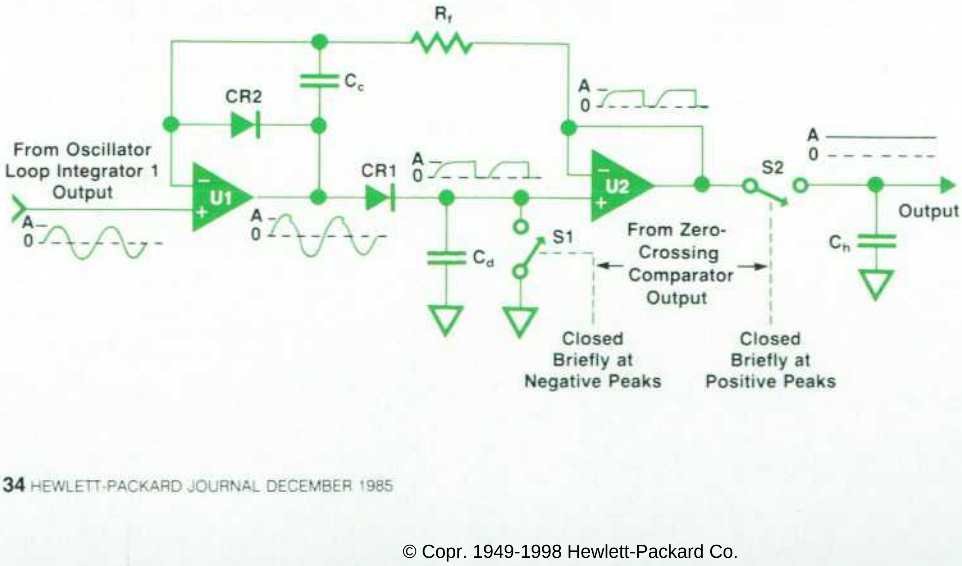


Fig. 6. *ALC loop peak detector.*

forward-biased, since two operational amplifiers are then involved in the feedback loop. At the negative peaks of the signal input, S1 is momentarily closed to discharge C_d, thus readying the detector to capture the next input peak.

The timing signals needed to drive S1 and S2 are derived from a zero-crossing comparator located at the output of the second oscillator loop integrator as shown in Fig. 5. At the frequency of oscillation, each oscillator loop integrator has unity gain and inverts and delays the phase of its input by 90 degrees. Therefore, zero crossings at an integrator's output correspond to peaks at its input, and the output of this comparator changes states on the peaks of the oscillator's output. The comparator's outputs are then differentiated to obtain 1-μs and 2-μs pulses which are used to drive the FET switches at the sample-and-hold peak detector.

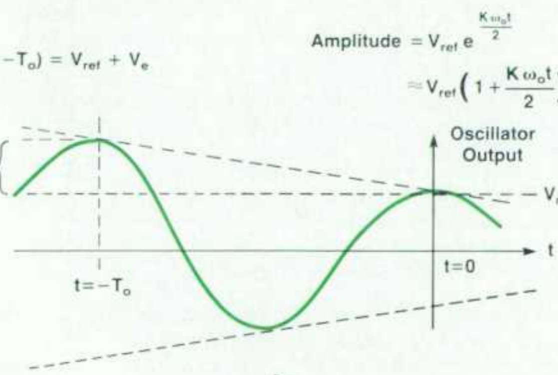
Once the oscillator output peak voltage has been obtained, it is subtracted from a fixed reference voltage in an error amplifier. The output of the error amplifier is zero volts when the oscillator amplitude has settled to the desired level. This voltage could be used directly as the control voltage for the oscillator loop's level setting analog multiplier except that the multiplier's control input is, in general, nonzero for a stable oscillator output amplitude.

At this point it is necessary to determine the optimum gain of the ALC loop to minimize oscillator setting time. To simplify analysis of the ALC loop's effect on the oscillator amplitudes, assume that the oscillator's peak output, V_p, is near its desired value, V_{ref}. From Fig. 4b, the oscillator output amplitude then becomes $V_p = V_{ref}\exp(K\omega_o t/2)$, where ω_o is the oscillator angular frequency and K is the analog multiplier gain. This is the voltage that appears at the output of the peak detector in Fig. 6 and is updated at every oscillator output peak. A further simplification in the analysis can be made by replacing V_p by its first-order approximation. By letting exp(x) be replaced by $1+x$, V_p becomes $V_{ref}\ (1+K\omega_o t/2)$.

Suppose the peak amplitude of the oscillator is sampled at time $t=-T_o$, T_o being the oscillator period, and suppose the sampled peak value V_p is equal to the desired value V_{ref} plus an error voltage V_e, as shown in Fig. 7. In the Fig. 5 block diagram, the output of the peak detector is $V_{ref}+V_e$, and the output of the error amplitude is V_e. For minimum

$V_p(t=-T_o) = V_{ref} + V_e$

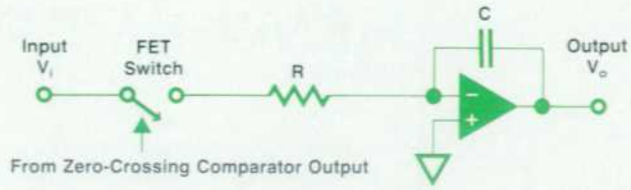
$$\text{Amplitude} = V_{ref}\, e^{\frac{K\omega_o t}{2}} \approx V_{ref}\left(1+\frac{K\omega_o t}{2}\right)$$



$$T_o = \text{Period} = \frac{2\pi}{\omega_o}$$

For minimum settling time, $\frac{K}{V_e} = \frac{-1}{\pi V_{ref}}$

Fig. 7. *Optimization of ALC loop gain.*



Switch is closed once at every oscillator peak.
Gate Time = T_g (Fixed).

$$\text{Gain per Oscillator Cycle} = \int_0^{T_g} \frac{-1}{RC}\,dt = \frac{-T_g}{RC}$$

$$\text{Steady-State Gain} = \left(\begin{array}{c}\text{Gain at}\\ \text{100\% Duty}\\ \text{Cycle}\end{array}\right) \times (\text{Duty Cycle})$$

$$= \frac{-1}{sRC}\frac{T_g}{T_o} = \frac{-1}{sRC}\frac{T_g\,\omega_o}{2\pi} \longleftarrow \text{Tracks oscillator frequency.}$$

Fig. 8. *Gated-gain ALC integrator.*

oscillator settling time, the ALC loop filter should transform this error voltage into a new analog multiplier gain K that will cause the ALC loop error voltage to be zero at the next oscillator output peak. In Fig. 7 this optimum loop filter gain is shown to be $G(s) = K/V_e = -1/\pi V_{ref}$. Note that this gain is both constant and independent of frequency.

To ensure oscillator level accuracy over frequency, the ALC loop filter must force the steady-state peak error voltage to zero. This is done by adding a low-frequency integrator to the loop filter response, as shown in Fig. 5. Both the ratio and sum of the integrator and pad gains can be chosen to set the total loop filter gain equal to the optimum gain to minimize oscillator settling time and to set the ALC loop phase margin to 60 degrees to minimize ALC loop peaking during oscillator settling. Since the optimum ALC loop gain is directly proportional to oscillator frequency, the ALC integrator gain must also increase directly with frequency if a constant phase margin is to be maintained. This is accomplished by using one of the fixed-length pulses generated by the oscillator's sample-and-hold-driving zero-crossing comparator to gate the ALC integrator's input. Since the pulse length is fixed and a pulse occurs once at every oscillator peak, the pulse duty cycle and thus the integrator gain increase directly with oscillator frequency. The circuit is shown in Fig. 8.

The result is a low-distortion audio oscillator with good level accuracy and minimum settling time over the required frequency range.

Reference

1. E. Vannerson and K.C. Smith, "A Low-Distortion Oscillator with Fast Amplitude Stabilization," *International Journal of Electronics*, Vol. 39, no. 4, 1975, pp. 465-472.

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4 — High-Performance Signal Generator

Robert E. Burns

Bob Burns is an R&D section manager who has been working on signal generators for HP since 1974. He was project manager for the HP 8642A/B and HP 8656A Signal Generators and also designed the output section for the HP 8656A. He was born in Philadelphia, Pennsylvania and has a BSEE degree awarded by Lehigh University in 1974. He has also done graduate work at Stanford University. Bob lives in Veradale, Washington and has two daughters. He likes camping, backpacking, boating, water skiing, snow skiing, and handball.

6 — User Interface and Controller

Albert Einstein Lassiter

With HP since 1979, Albert Lassiter designed and developed the user interface and HP-IB hardware and firmware for the HP 8642A/B Signal Generators. He has also worked on the HP 8902A Measuring Receiver and the HP 8350A Sweep Oscillator, among other products. He is currently responsible for firmware architecture and development and for user interfaces for a new product line. He graduated from the University of California at Berkeley with a BS degree in electrical engineering and computer science in 1979. A resident of Liberty Lake, Washington, Albert is married and has two sons. He's a jazz trumpet player, composer, arranger, and teacher. Every Christmas season he organizes a group of horn players who entertain others with jazzy Christmas carols.

Charles R. Kogler

Chuck Kogler was born in Milwaukee, Wisconsin and completed work for a BS degree in electrical and computer engineering from the University of Wisconsin at Madison in 1979. With HP since 1980, he designed controller hardware and internal control firmware for the HP 8642A/B Signal Generators. He is named coinventor on a patent application related to those products and is working toward an MSEE degree from the University of Idaho. He's a resident of Liberty Lake, Washington, is married, and has two daughters. He likes spending time with his family and enjoys making beer, watching films, and golfing.

10 — Signal Generator Service

Michael T. Wende

Born in Houston, Texas, Mike Wende completed work for a BSEE degree from the University of Texas at Arlington in 1980. After joining HP the same year he worked on test systems and serviceability for the HP 8642A/B Signal Generators. His professional interests include embedded system design and support design and he teaches electrical engineering at Gonzaga University. Mike and his wife live in Spokane, Washington. His hobbies include motorcycling, camping, operating radio-controlled models, and programming his home computer.

14 — Mechanical Design

Mark W. Johnson

With HP since 1979, Mark Johnson contributed to the mechanical design of the HP 8663 and HP 8642A/B Signal Generators. He is named coinventor on a patent application related to modular product design and is interested in computer-aided design. Mark was born in Burbank, California and holds a BSME degree awarded in 1979 by the University of California at Santa Barbara. He's a resident of Liberty Lake, Washington and just returned from a one-year tour of western Europe, Turkey, and Yugoslavia. He enjoys backpacking, kayaking, bicycle touring, all kinds of skiing, and plays volleyball on a nationally ranked team. He also contributes some spare time to the physics department of a local high school.

Michael B. Jewell

Mike Jewell started at HP in 1976 as an R&D product design engineer. He was the mechanical designer of the HP 3586A/B Selective Level Meter and was codesigner of the HP 8642A/B Signal Generators. He is currently working on software and productivity tools. He is named coinventor on two patent applications, one on a backlight for liquid crystal displays and the other on modular product design. He was born in Norfolk, Virginia and served in the U.S. Army before earning a BSME degree from the University of Maryland in 1975. He lives with his wife and two children in Spokane, Washington and likes photography, astronomy, and backpacking.

18 — Output Section

Bryan D. Ratliff

Born in Bitburg, Germany, Bryan Ratliff earned a BSEE degree from the University of California at Davis in 1981. He joined HP the same year and was responsible for the frequency doubler output section of the HP 8642B Signal Generator. Bryan lives in Spokane, Washington, is married, and has a young daughter. He is a member of the Hunger Project. A new homeowner, he enjoys being able to grow his own garden and also likes fishing, camping, and skiing.

Marvin W. Wagner

Marv Wagner has been with HP since 1981 and was responsible for portions of the output section design of the HP 8642A/B Signal Generators. He is presently an R&D productivity manager and is interested in computer graphics and CAD/CAE tools. He was born in Salt Lake City, Utah and attended the University of Utah, earning a BSEE degree in 1981. Marv, his wife, and four children live in Spokane, Washington. He is involved in youth activities and sports in his church and likes playing softball and basketball.

Robert R. Collison

With HP since 1973, Bob Collison was project manager for the output section of the HP 8642A/B Signal Generators. He has also contributed to the development of the HP 8654B Signal Generator, the HP 8901A Modulation Analyzer, and the HP 7910, HP 7911, and HP 7912 Disc Drives. He was born in Yakima, Washington, completed work for a BSEE degree from Washington State University in 1971, and went on to earn an MSEE degree from the University of Washington in 1973. Bob, his wife, and his son live in Veradale, Washington. He likes camping, boating, all types of skiing, and working on home improvement projects.

James B. Summers

Jim Summers was born in Michigan City, Indiana and educated at the University of Wisconsin at Madison. He earned his BSEE degree in 1978 and his MSEE degree in 1979, coming to HP the same year. He designed the UHF output section for the HP 8642A/B Signal Generators, reverse power protection for the HP 8642B, and the attenuator interface for the HP 8642A. He lives in Spokane, Washington, is an amateur radio operator (KD7F), and likes tinkering with radio-controlled models. He also enjoys golf, tennis, hunting, and fishing.

24 Frequency Synthesizer

Earl C. Herleikson

Earl Herleikson is a native of Spokane, Washington and a graduate of the University of California at Davis (BSEE 1980). After joining HP in 1980 he worked on the development of the HP 8642A/B Signal Generators. He is interested in low-noise RF design. Earl is married, has four children, and is a Boy Scout troop leader. When not working on his ranch near Spokane, he enjoys windsurfing.

Ronald J. Mayer

With HP since 1981, Ron Mayer contributed to the development of the SAWR loop and 45-MHz time base for the HP 8642A/B Signal Generators. He was born in Long Beach, California and received his BSEE degree from California Polytechnic State University at Pomona in 1981. He also served in the U.S. Navy as an electronics technician. Ron is married, has one son, and lives in Veradale, Washington. He likes skiing, gardening, and toying with radio-controlled model helicopters.

Brian M. Miller

With HP since 1979, Brian Miller is a project manager at the Spokane Division. He has worked on the HP 8956A System Interface and designed the FM loop and the counter for the HP 8642A/B Signal Generators. He was a project manager for the HP 8903B/E Audio Analyzers and is the coinventor on several patent applications. Brian was brought up in Littleton, Colorado and attended the University of Colorado (BSEE 1979). He lives in Spokane, Washington with his wife and has served on a city/county task force working on local problems. He is an avid birdwatcher and is an amateur radio operator with an Extra Class license (NI7P). He also likes fishing, hiking, and working on cars.

Mark A. Niemann

A 1979 graduate of the University of Wisconsin at Madison, Mark Niemann has a BSEE degree. After joining HP in 1979 he contributed to the development of the HP 8902A Measuring Receiver and the HP 8903B/E Audio Analyzers. More recently he worked on the power supply and IF reference for the HP 8642A/B Signal Generators. Mark was born in Watertown, Wisconsin and now lives in Liberty Lake, Washington. He lists skiing, playing the piano, photography, and working in the darkroom as outside interests.

Thomas R. Faulkner

An R&D engineer at HP's Spokane Division, Tom Faulkner has been with HP since 1979. He worked on the HP 8656A Signal Generator and contributed to the development of the sum and reference loops and production pretest station for the HP 8642A/B Signal Generators. He is presently investigating the feasibility of a new product. An alumnus of the University of California at Davis, he earned a BSEE degree in 1976 and an MSEE degree in 1978. Tom was born in Sacramento, California and now lives in Spokane, Washington with his wife and three children. He has developed exhibits for the Eastern Washington University Science Center and is interested in alternate energy design for homes. His other outside interests include electronics, woodworking, photography, and playing the piano.

31 Audio Modulation

Gary L. Tong

Gary Tong completed work for a BSEE degree from Case Western Reserve University in 1980 and came to HP the same year. He designed the modulation section and heterodyne reference for the HP 8642A/B Signal Generators and the firmware for the HP 8903B/E Audio Analyzers. His professional interests include circuit and system design, audio and RF, and digital firmware and hardware. Gary was born in Tiffin, Ohio and currently is a resident of Spokane, Washington. He is an an amateur radio operator (N7CDT) and enjoys skiing, hiking, astronomy, and home computers.

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